3.3V CMOS 16-BIT LATCHED TRANSCEIVER

IDT74FCT163543A/C

FEATURES:

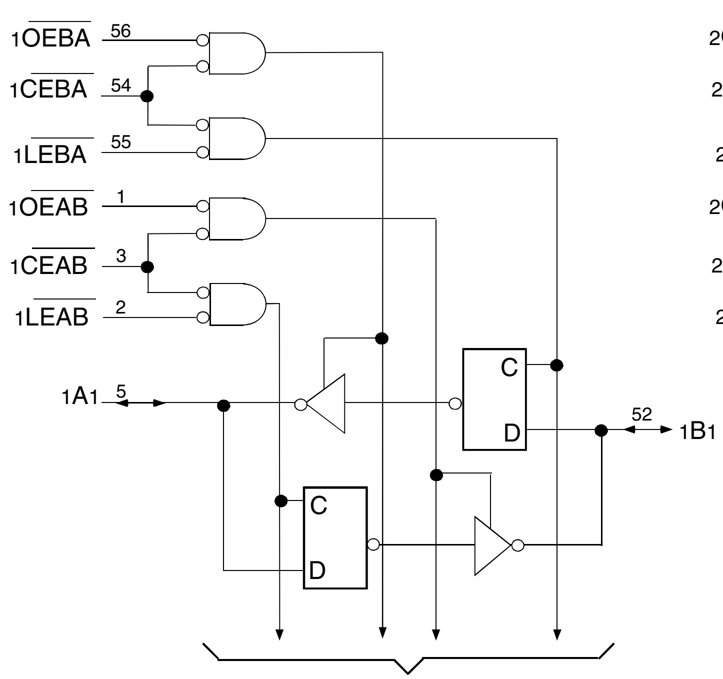
- **0.5 MICRON CMOS Technology**
- **Typical tSK(o) (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **VCC = 3.3V ± 0.3V, Normal Range, or VCC = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-rail output swing for increased noise margin**
- **Low Ground Bounce (0.3V typ.)**
- **Inputs (except I/O) can be driven by 3.3V or 5V components**
- **Available in SSOP and TSSOP packages**

DESCRIPTION:

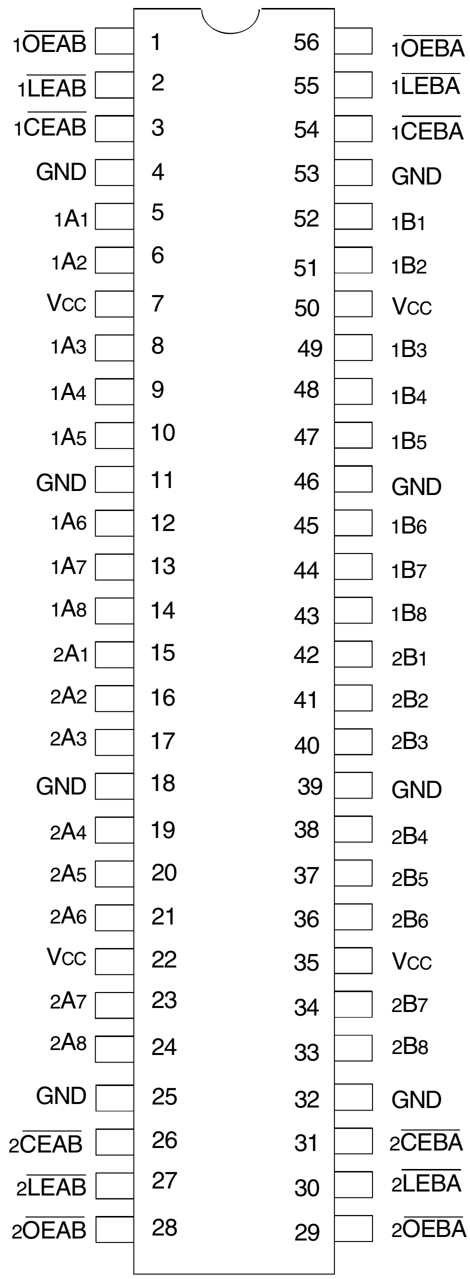
The FCT163543 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable (x$\overline{CEAB}$) must be low in order to enter data from the A port or to output data from the B port. x$\overline{LEAB}$ controls the latch function. When x$\overline{LEAB}$ is low, the latches are transparent. A subsequent low-to-high transition of x$\overline{LEAB}$ signal puts the A latches in the storage mode. x$\overline{OEAB}$ performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using x$\overline{CEBA}$, x$\overline{LEBA}$, and x$\overline{OEBA}$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163543 have series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xOEAB	A-to-B Output Enable Input (Active LOW)
xOEBA	B-to-A Output Enable Input (Active LOW)
xCEAB	A-to-B Enable Input (Active LOW)
xCEBA	B-to-A Enable Input (Active LOW)
xLEAB	A-to-B Latch Enable Input (Active LOW)
xLEBA	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
VTERM(3)	Terminal Voltage with Respect to GND	–0.5 to 7	V
VTERM(4)	Terminal Voltage with Respect to GND	–0.5 to VCC+0.5	V
TSTG	Storage Temperature	–65 to +150	°C
IOUT	DC Output Current	–60 to +60	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Outputs and I/O terminals.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COUT	Output Capacitance	VOUT = 0V	3.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(1, 3)

FOR A-TO-B (SYMMETRIC WITH B-TO-A)

Inputs			Latch Status	Output Buffers
xCEAB	xLEAB	xOEAB	xAx to xBx	xBx
H	X	X	Storing	Z
X	H	X	Storing	X
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous(2) A Inputs
L	L	H	Transparent	Z
L	H	H	Storing	Z

NOTES:
1. A-to-B data flow shown; B-to-A flow control is the same, except using xCEBA, xLEBA and xOEBA.
2. Before xLEAB LOW-to-HIGH Transition
3. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	5.5	V
	Input HIGH Level (I/O pins)			2	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}-0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3	—	
		V_{CC} = 3V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.4[5]	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	—	—	0.2	V
			I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.1	10	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC}–0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = V_{CC} - 0.6V$[3]		—	2	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $x\overline{CEAB}$ and $x\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	60	100	µA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$ and $x\overline{OEAB}$= GND $x\overline{CEBA}$ = V_{CC} One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	—	0.6	1	mA
			$V_{IN} = V_{CC} - 0.6V$ V_{IN} = GND	—	0.6	1	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$ and $x\overline{OEAB}$= GND $x\overline{CEBA}$ = V_{CC} Sixteen Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	—	2.4	4[5]	
			$V_{IN} = V_{CC} - 0.6V$ V_{IN} = GND	—	2.4	4.3[5]	

NOTES:

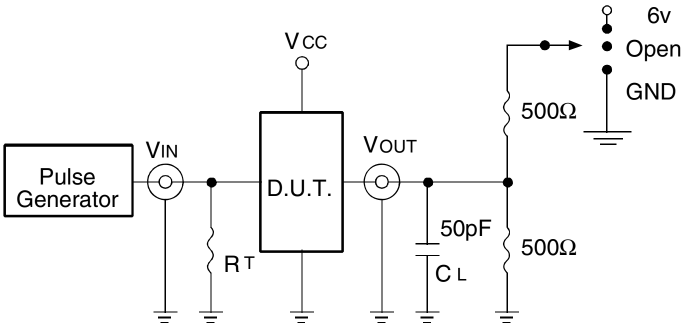
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[1]

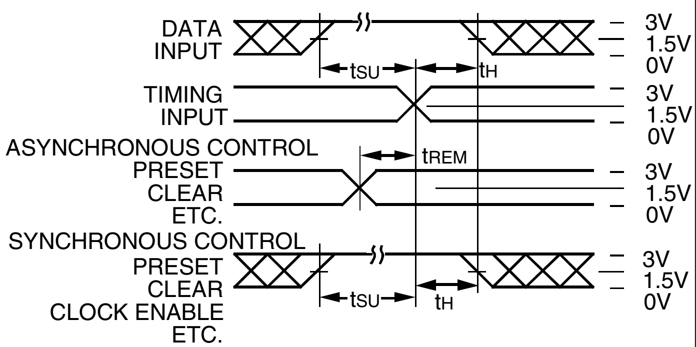
Symbol	Parameter	Condition[2]	FCT163543A		FCT163543C		Unit
			Min.[3]	Max.	Min.[3]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.3	ns
t_{PLH} t_{PHL}	Propagation Delay x$\overline{\text{LEBA}}$ to xAx, x$\overline{\text{LEAB}}$ to xBx		1.5	8	1.5	7	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{\text{OEBA}}$ or x$\overline{\text{OEAB}}$ xAx or xBx x$\overline{\text{CEBA}}$ or x$\overline{\text{CEAB}}$ xAx or xBx		1.5	9	1.5	8	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{\text{OEBA}}$ or x$\overline{\text{OEAB}}$ xAx or xBx x$\overline{\text{CEBA}}$ or x$\overline{\text{CEAB}}$ xAx or xBx		1.5	7.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW xAx or xBx to x$\overline{\text{LEAB}}$ or x$\overline{\text{LEBA}}$		2	—	2	—	ns
t_H	Hold Time HIGH or LOW xAx or xBx to x$\overline{\text{LEAB}}$ or x$\overline{\text{LEBA}}$		2	—	2	—	ns
t_W	x$\overline{\text{LEBA}}$ or x$\overline{\text{LEAB}}$ Pulse Width LOW		5	—	5	—	ns
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	ns

NOTES:
1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

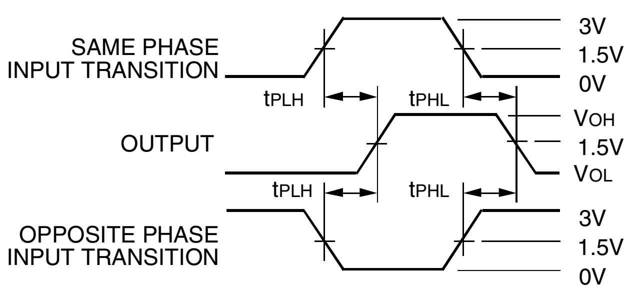
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times

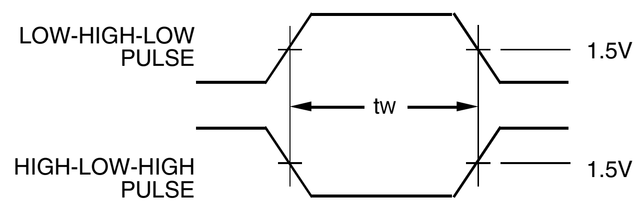


Propagation Delay

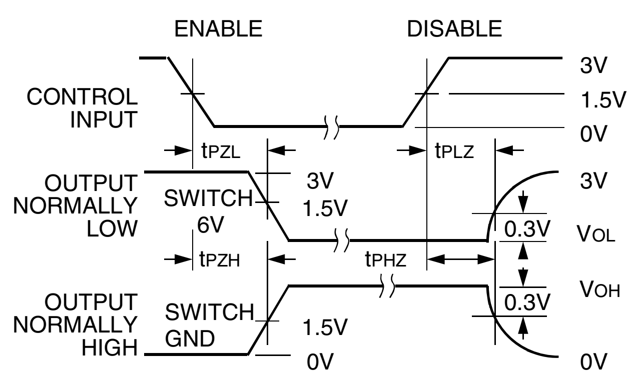
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. if V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION

IDT XX FCT XXX XXXX X

(XX = Temp. Range, XXX = Family, XXXX = Device Type, X = Package)

Package	PV	Shrink Small Outline Package
	PA	Thin Shrink Small Outline Package
Device Type	543A	16-Bit Latched Transceiver
	543C	
Family	163	Double-Density 3.3Volt
Temp. Range	74	– 40°C to +85°C

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
logichelp@idt.com