P54/74PCT821A/B–P54/74PCT823A/B P54/74PCT825A/B BUS INTERFACE REGISTERS

PRELIMINARY

T-52-07

FEATURES

- Equivalent to Bipolar Am29821/23/25 Bipolar Registers
- Full CMOS Implementation
- Low Power Operation
- Fully TTL Compatible Input and Output Levels
- High Speed Parallel Registers with positive edge-triggered D-type Flip-Flops
- Buffered Common Clock Enable ($\overline{EN}$) and Asynchronous Clear Input ($\overline{CLR}$)
- I_{OL} = 48mA (Commercial) and 32mA (Military)
- Clamp Diodes on all Inputs for Ringing Suppression
- Compact Pinout
  - 24-Pin 300 mil DIP, SOIC
  - 28-Pad 450 mil sq. LCC

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DESCRIPTION

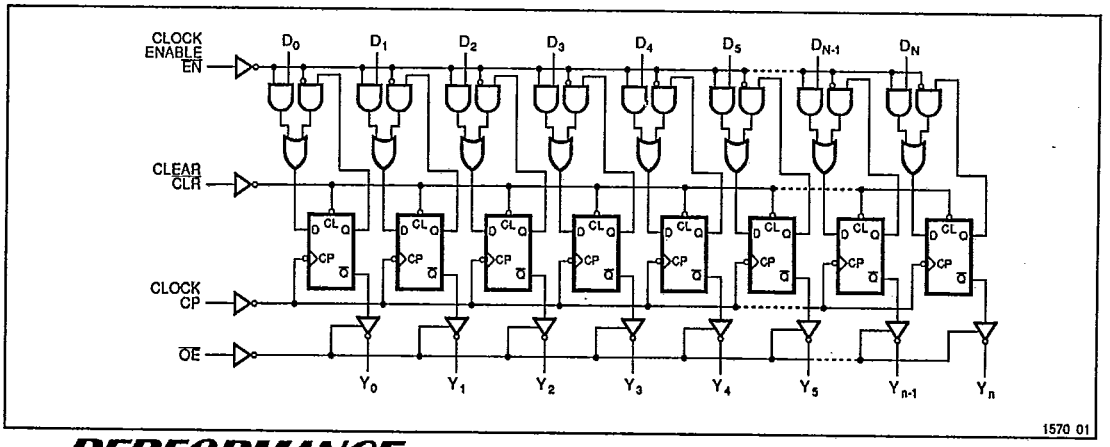
The P54/74PCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The P54/74PCT821 is a buffered, 10 bit wide version of the popular '374 function. The P54/74PCT823 is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance microprogrammed systems. The P54/74PCT825 is a 8-bit buffered register with all the 'PCT823 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

The P54/74PCT800 family of devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The P54/74PCT820 interface family is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picosecond at room temperature and 5.0V.

FUNCTIONAL BLOCK DIAGRAM



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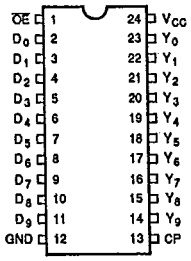
PRODUCT SELECTOR GUIDE

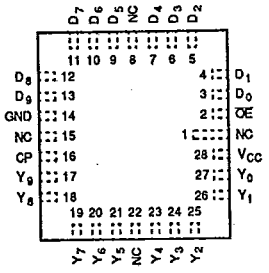
	Device		
Non-Inverting	10-Bit	9-Bit	8-Bit
	54/74PCT821A/B	54/74PCT823A/B	54/74PCT825A/B

PIN CONFIGURATONS

P54/74PCT821 (10-Bit Register)

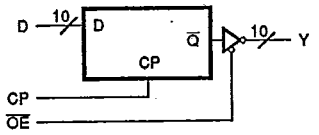


DIP (D4,P4) SOIC (S4)



LCC (L5-1)

LOGIC SYMBOLS



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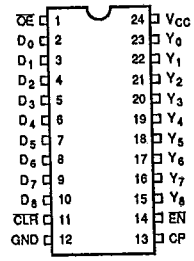
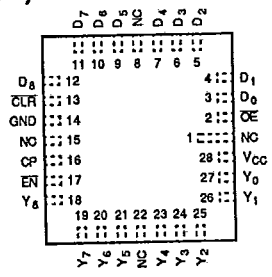
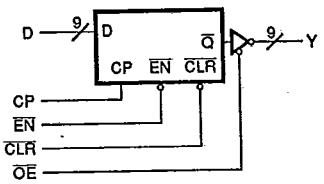
P54/74PCT823 (9-Bit Register)



DIP (D4,P4) SOIC (S4)

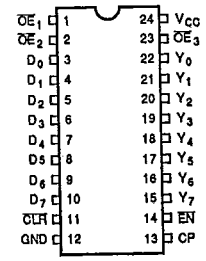


LCC (L5-1)

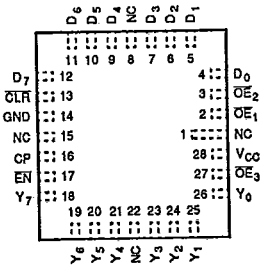


1570 03

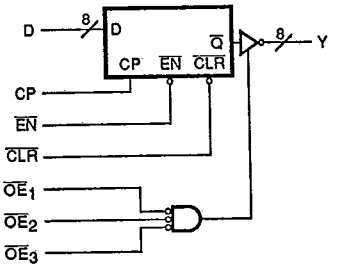
P54/74PCT825 (8-Bit Register)



DIP (D4,P4) SOIC (S4)



LCC (L5-1)



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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage				–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2			V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2			V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –15mA
		Commercial (TTL)	2.7			V	MIN	I_{OH} = –24mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V			0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)			0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)			0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)			0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied				10	µA	MAX	V_{OUT} = V_{CC}
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied				–10	µA	MAX	V_{OUT} = GND
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied[3]				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied[3]				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–75			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

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DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CCQC}	Quiescent Power Supply Current (CMOS inputs) Com'l. / Mil.	.003 / .003	0.3 / 0.5	mA / mA	V_{CC} = MAX, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$, f = 0, Outputs Open
I_{CCQT}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$, Outputs Open
I_{CC}	Total Power Supply Current[5]		4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
			6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND
			7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
			16.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CCQC} = Quiescent Current with CMOS input levels
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

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AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	P54/74PCT821A/823A/825A				P54/74PCT821B/823B/825B				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	– –	12.0 12.0	– –	12.0 12.0	– –	8.5 8.5	– –	7.5 7.5	ns ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)	C_L = 300pF[2] R_L = 500Ω	– –	20.0 20.0	– –	20.0 20.0	– –	16.0 16.0	– –	15.0 15.0	ns ns	1, 5
t_{PLH}	Propagation Delay Clear to Y_i	C_L = 50pF R_L = 500Ω	–	20.0	–	20.0	–	9.5	–	9.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_i ↑	C_L = 50pF R_L = 500Ω	– –	15.0 15.0	– –	14.0 14.0	– –	9.0 9.0	– –	8.0 8.0	ns ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_i ↑	C_L = 300pF[2] R_L = 500Ω	– –	25.0 25.0	– –	23.0 23.0	– –	16.0 16.0	– –	15.0 15.0	ns ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_i ↑	C_L = 5pF[2] R_L = 500Ω	– –	10.0 10.0	– –	9.0 9.0	– –	7.0 7.0	– –	6.5 6.5	ns ns	1, 7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_i ↑	C_L = 50pF R_L = 500Ω	– –	18.0 18.0	– –	16.0 16.0	– –	8.0 8.0	– –	7.5 7.5	ns ns	1, 7, 8

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AC OPERATING REQUIREMENTS

Symbol	Parameter	Test Conditions	P54/74PCT821A/823A/825A				P54/74PCT821B/823B/825B				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{SU}	Data to CP Set-up Time	C_L = 50pF R_L = 500Ω	4.0	–	4.0	–	3.0	–	3.0	–	ns	4
t_h	Data CP Hold Time		2.0	–	2.0	–	1.5	–	1.5	–	ns	4
t_{su}	Enable ($\overline{EN}$ ↑) to CP Set-up Time		4.0	–	4.0	–	3.0	–	3.0	–	ns	9
t_h	Enable $\overline{EN}$ Hold Time		2.0	–	2.0	–	0.0	–	0.0	–	ns	9
t_{rec}	Clear Recovery ($\overline{CLR}$ ↑) Time		7.0	–	7.0	–	6.0	–	6.0	–	ns	6
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW		7.0 7.0	– –	7.0 7.0	– –	6.0 6.0	– –	6.0 6.0	– –	ns ns	5
$t_w(L)$	Clear ($\overline{CLR}$ = LOW) Pulse Width		7.0	–	7.0	–	6.0	–	6.0	–	ns	5

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Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These parameters are guaranteed but not tested.

PIN DESCRIPTION

Name	I/O	Description
D_1	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_1 outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	O	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
$Y_1, \overline{Y}_1$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_1 input is transferred to the Q_1 output on the LOW-to HIGH clock transition. When the clock enable is HIGH, the Q_1 outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_1 outputs are in the high impedence state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_1 outputs.

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FUNCTION TABLES T-52-07

P54/74PCT821/23/25

Inputs					Internal Outputs		Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_1	CP	Q_1	Y_1	
H	X	L	L	↑	L	Z	High Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH, L = LOW, X = Don't Care, NC = No Change, 1570 Tbl 10
↑ = LOW-to-HIGH Transition, Z = HIGH Impedance

ORDERING INFORMATION

PxxPCT (Temp. Class) / xxxx (Device type) / x (Package) / x (Temperature) / x (Processing)

Processing	
B	MIL-STD-883, Class B
Temperature	
C	0°C to +70°C
M	–55°C to +125°C
Package	
P	Plastic DIP
D	CERDIP
S	Small Outline IC
L	Leadless Chip Carrier
Device type	
821A	10-Bit Non-Inverting Register
821B	Fast 10-Bit Non-Inverting Register
823A	9-Bit Non-Inverting Register
823B	Fast 9-Bit Non-Inverting Register
825A	8-Bit Non-Inverting Register
825B	Fast 8-Bit Non-Inverting Register
Temp. Class	
74	Commercial
54	Military

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TECHDOC 1570