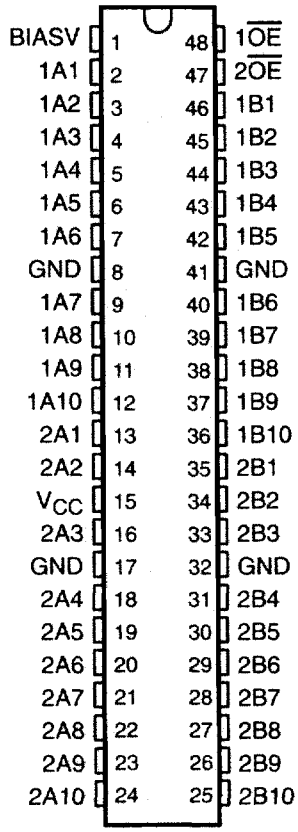
CBTLV16215
LOW-VOLTAGE 20-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS

SCDS045A – DECEMBER 1997 – REVISED MARCH 1998

- **5-Ω Switch Connection Between Two Ports**
- **Isolation Under Power-Off Conditions**
- **B-Port Outputs are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The CBTLV16215 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The device is organized as dual 10-bit bus switches with separate output-enable ($\overline{OE}$) inputs. It can be used as two 10-bit bus switches or one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, a high-impedance state exists between the two ports, and port B is precharged to BIASV through the equivalent of a 10-kΩ resistor.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CBTLV16215 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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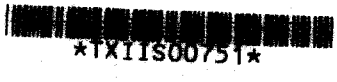
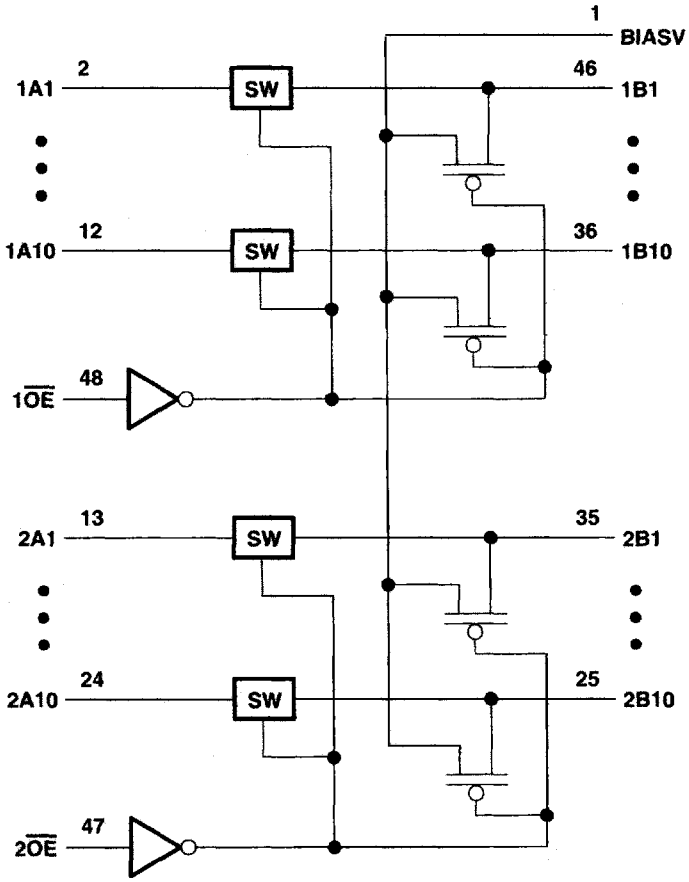
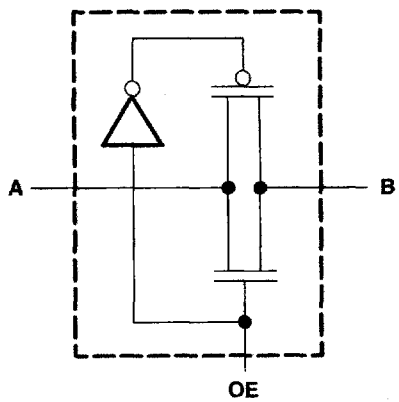


logic diagram



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Bias voltage range, BIASV ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package ..... 89°C/W
DGV package ..... 93°C/W
DL package ..... 94°C/W
Storage temperature range, T_{stg} ..... –65 C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratin s only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating condit ons" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observ d.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
BIASV	Bias voltage		0	V_{CC}	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±5	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	µA
I_O		V_{CC} = 3 V,	BIASV = 2.4 V,	V_O = 0	0.25			mA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	µA
ΔI_{CC}§	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			500	µA
C_i	Control inputs	V_I = 3 V or 0						pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off					pF
r_{on}¶		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA				Ω
				I_I = 24 mA				
			V_I = 1.7 V,	I_I = 15 mA				
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA				
				I_I = 24 mA				
			V_I = 2.4 V,	I_I = 15 mA				

‡ All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

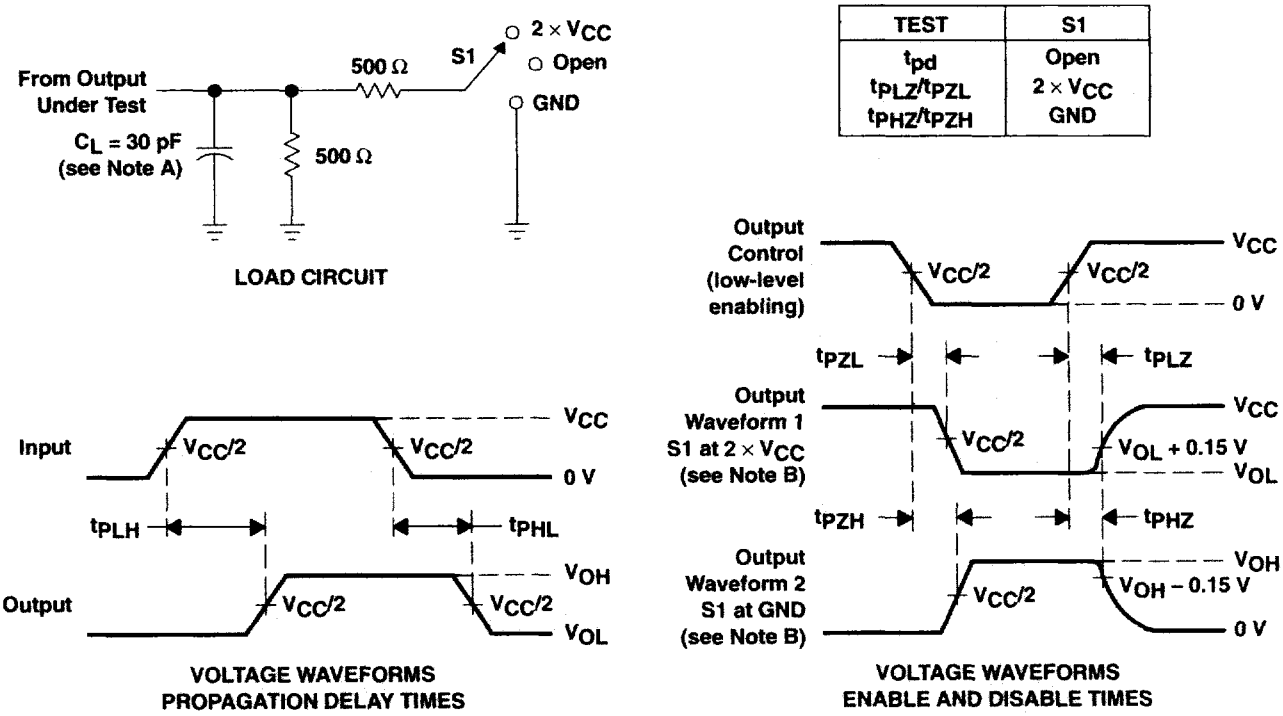
PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}†		A or B	B or A					ns
t_{PZH}	BIASV = GND	$\overline{OE}$	A or B					ns
t_{PZL}	BIASV = 3 V							
t_{PHZ}	BIASV = GND	$\overline{OE}$	A or B					ns
t_{PLZ}	BIASV = 3 V							

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified lo d capacitance, when driven by an ideal voltage source (zero output impedance).

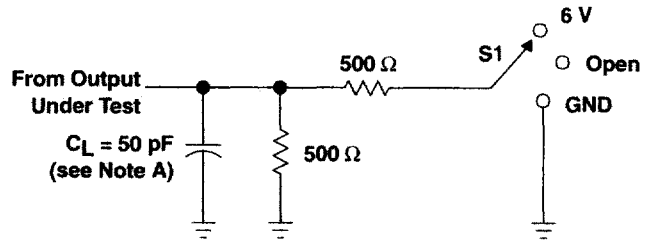
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

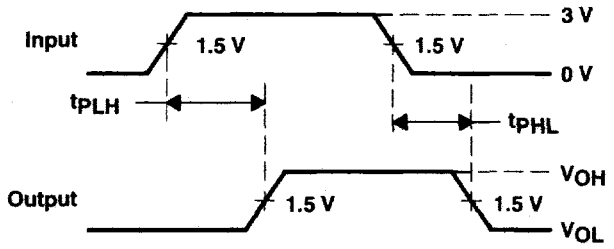
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V

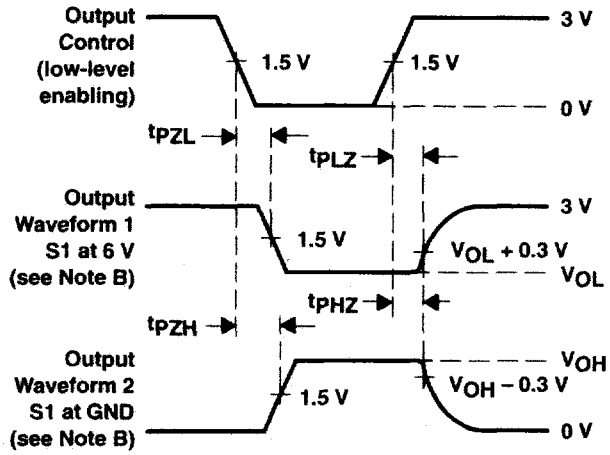


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms