



## 24-BIT BUS EXCHANGE SWITCH

**IDT74FST163212**

### FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance;  $4\Omega$
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in SSOP and TSSOP packages

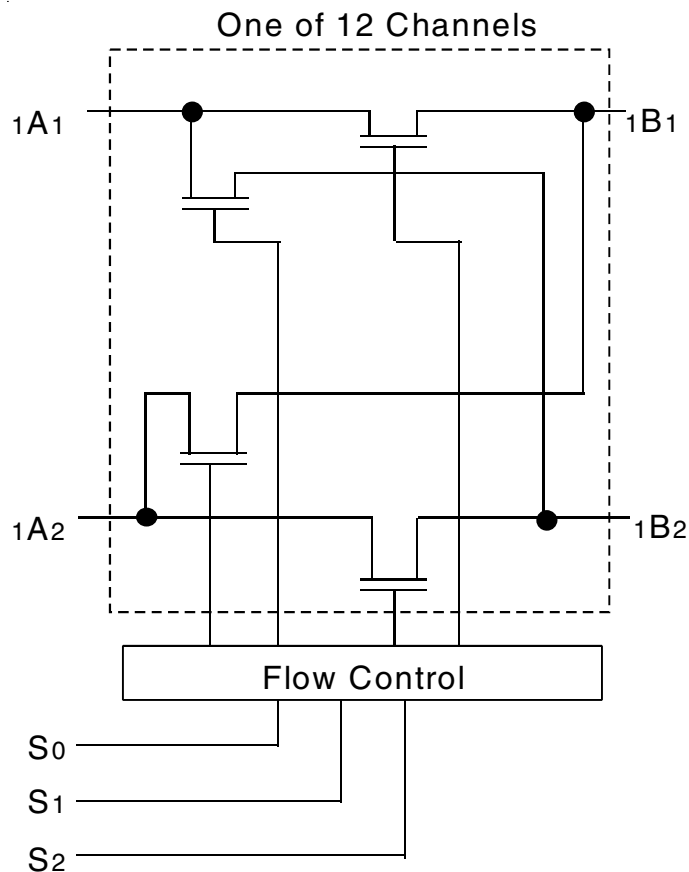
### DESCRIPTION:

The FST163212 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

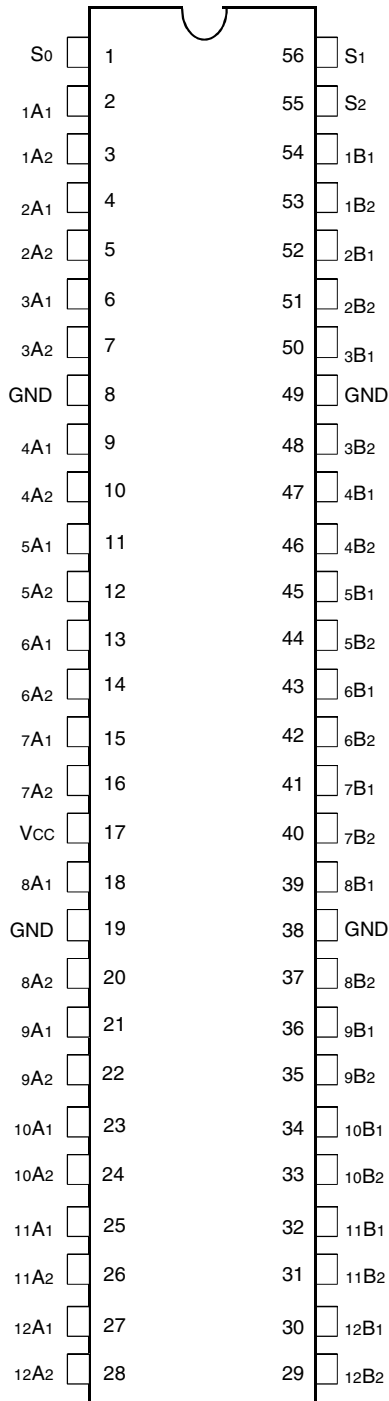
The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST163212 provides four 12-bit TTL-compatible ports that support 2 way bus exchange. The So-2 pins control the bus exchange and switch enable functions.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	Maximum Continuous Channel Current	128	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub>, Control, and Switch terminals.

## CAPACITANCE<sup>(1)</sup>

Symbol	Parameter	Conditions <sup>(2)</sup>	Typ.	Unit
C <sub>IN</sub>	Control Input Capacitance		6	pF
C <sub>I/O</sub>	Switch Input/Output Capacitance	Switch Off	17	pF

### NOTES:

- Capacitance is characterized but not tested.
- T<sub>A</sub> = 25°C, f = 1MHz, V<sub>IN</sub> = 0V, V<sub>OUT</sub> = 0V.

## PIN DESCRIPTION

Pin Names	I/O	Description
A1, A2 B1, B2	I/O	Buses A1, A2, B1, B2
S0-2	I	Control Pins for MUX and Switch Enable Functions

## FUNCTION TABLE<sup>(1)</sup>

S2	S1	S0	A1	A2	Description
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 to B1
L	H	L	B2	Z	A1 to B2
L	H	H	Z	B1	A2 to B1
H	L	L	Z	B2	A2 to B2
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 to B1, A2 to B2
H	H	H	B2	B1	A1 to B2, A2 to B1

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Control Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
$V_{IL}$	Control Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
$I_{IH}$	Control Input HIGH Current	$V_{CC} = \text{Max.}$ $V_i = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Control Input LOW Current		$V_i = \text{GND}$	—	—	
$I_{OZH}$	Current During	$V_{CC} = \text{Max.}, V_o = 0$ to $5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$	Bus Switch Disconnect		—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
$I_{OFF}$	Switch Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN}$ or $V_o \leq 5.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or $V_{CC}$	—	0.1	3	$\mu\text{A}$

## BUS SWITCH IMPEDANCE OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$R_{ON}$	Switch On Resistance <sup>(2)</sup>	$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 64\text{mA}$	—	4	7	$\Omega$
		$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 30\text{mA}$	—	4	7	
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$	—	10	15	
$I_{OS}$	Short Circuit Current, A to B <sup>(3)</sup>	$A(B) = 0\text{V}, B(A) = V_{CC}$	100	—	—	$\text{mA}$

### NOTES:

1. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
2. The voltage drop between the indicated ports divided by the current through the switch.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4,5)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Select Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	30	40	$\mu A/$ MHz/ Switch
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Select Pins Toggling (24 Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	7.2	9.6	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	7.7	11.1	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $GND$ . Switch inputs do not contribute to  $\Delta I_{CC}$ .
- This parameter represents the current required to switch the internal capacitance of the control inputs at the specified frequency. Switch inputs generate no significant power supply currents as they transition. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- $C_{PD} = I_{CCD}/V_{CC}$   
 $C_{PD}$  = Power Dissipation Capacitance
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_i$  = Control Input Frequency  
 $N$  = Number of Control Inputs Toggling at  $f_i$

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

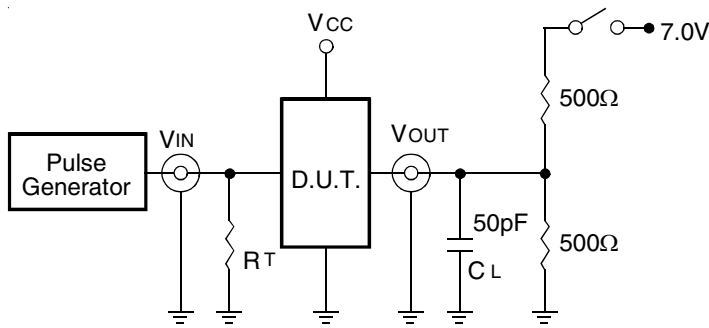
Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0V \pm 10\%$

Symbol	Description <sup>(1)</sup>	$V_{CC} = 5V \pm 10\%$			$V_{CC} = 4V$	Unit
		Min.	Typ.	Max.	Max.	
$t_{PLH}$ $t_{PHL}$	Data Propagation Delay A to B, B to A <sup>(2)</sup>	—	—	0.25	0.25	ns
$t_{BX}$	Switch Multiplex Delay S to A, B	1.5	—	6.5	7	ns
$t_{PZH}$ $t_{PZL}$	Switch Turn On Delay S to A, B	1.5	—	6.5	7	ns
$t_{PHZ}$ $t_{PLZ}$	Switch Turn Off Delay S to A, B	1.5	—	7	7	ns
$ Q_{C1} $	Charge Injection During Switch DISCONNECT S to A or B <sup>(3)</sup>	—	1.5	—	—	pC
$ Q_{DC1} $	Charge Injection During Switch Exchange S to A or B <sup>(3)</sup>	—	0.5	—	—	pC

### NOTES:

- See test circuits and waveforms.
- The bus switch contributes no Propagation Delay other than the RC Delay of the load interacting with the RC of the switch.
- $|Q_{C1}|$  is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers.  $|Q_{DC1}|$  is the charge injection for a multiplexer as the multiplexed port switches from one path to another. Charge injection is reduced because the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

TEST CIRCUITS AND WAVEFORMS



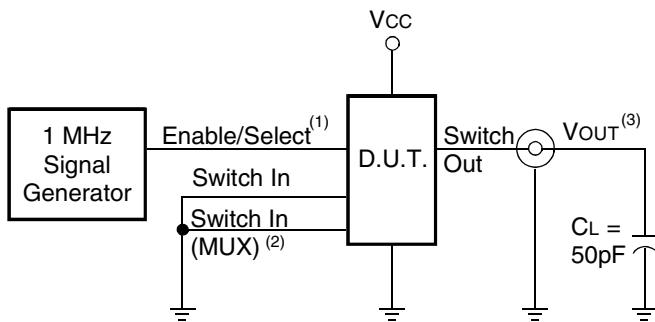
Test Circuits for All Outputs

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

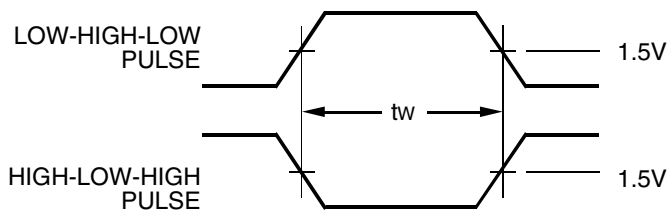
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



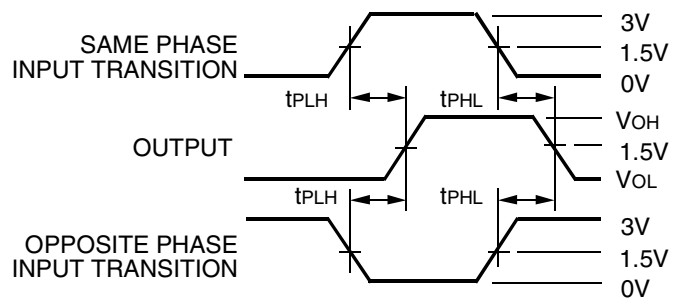
Charge Injection

NOTES:

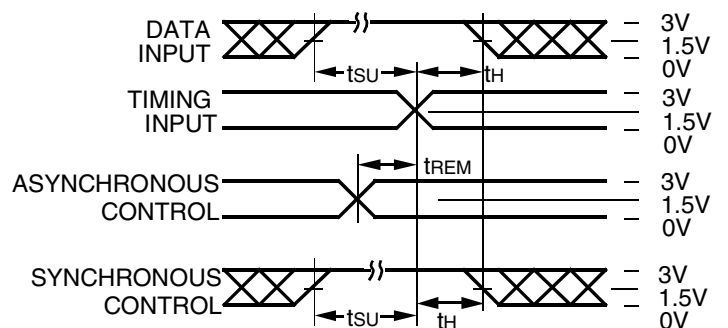
- Select is used with multiplexers for measuring IQocil during multiplexer select. During all other tests Enable is used.
- Used with multiplexers to measure IQocil only.
- Charge Injection =  $\Delta V_{out} C_L$ , with Enable toggling for IQocil or Select toggling for IQocil.  $\Delta V_{out}$  is the change in Vout and is measured with a 10MΩ probe.



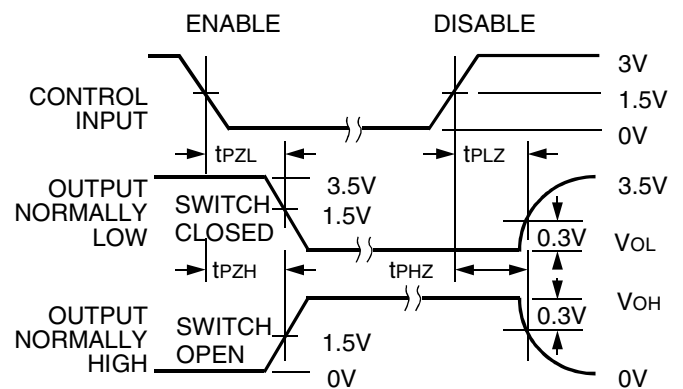
Pulse Width



Propagation Delay



Set-up, Hold, and Release Times

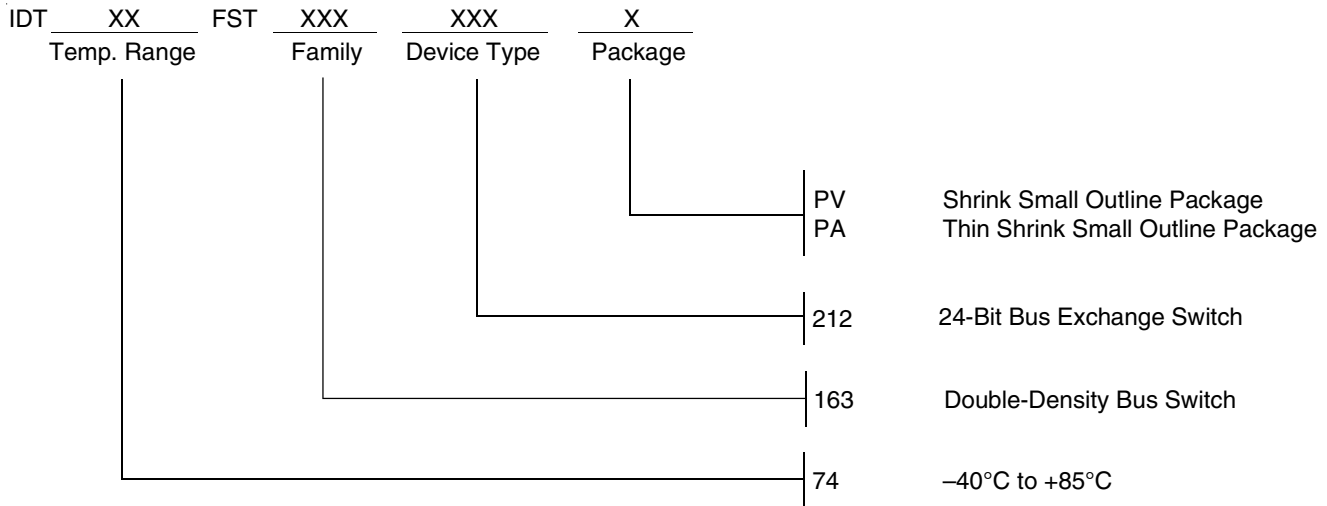


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



## DATA SHEET DOCUMENT HISTORY

5/24/2002 Removed TVSOP package



**CORPORATE HEADQUARTERS**  
2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**  
800-345-7015 or 408-727-6116  
fax: 408-492-8674  
www.idt.com

**for Tech Support:**  
logichelp@idt.com  
(408) 654-6459