National Semiconductor

T-67-21-55

MM54HC137/MM74HC137 3-to-8 Line Decoder With Address Latches (Inverted Output)

General Description

This device utilizes advanced silicon-gate CMOS technology, to implement a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

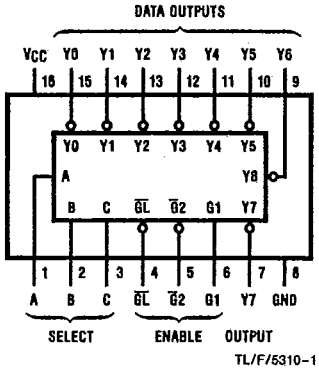
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing.
- Fanout of 10 LS-TTL loads.

Connection and Functional Block Diagrams

Dual-In-Line Package



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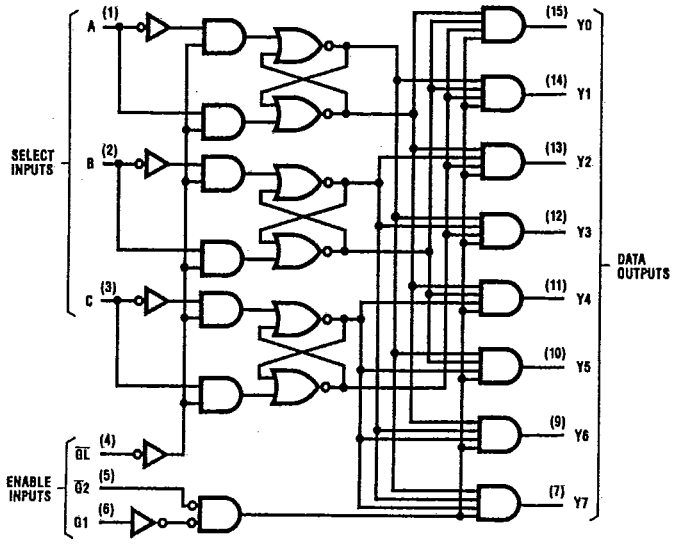
Order Number MM54HC137* or MM74HC137*

*Please look into Section 8, Appendix D for availability of various package types.



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

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AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		14	29	ns
t_{PHL}	Maximum Propagation Delay, A, B or C to any Y Output		20	42	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		12	22	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		15	34	ns
t_{PLH}	Maximum Propagation Delay G1 to any Output		13	25	ns
t_{PHL}	Maximum Propagation Delay GL to any Output		17	34	ns
t_{PLH}	Maximum Propagation GL to Output		15	30	ns
t_{PHL}	Maximum Propagation Delay GL to Output		22	34	ns
t_S	Minimum Setup Time at A, B and C Inputs			20	ns
t_H	Minimum Hold Time at A, B and C Inputs			0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C		54HC $T_A=-55$ to 125°C		Units
				Typ	Guaranteed Limits				
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		2.0V 4.5V 6.0V	85 17 14	170 34 29		214 43 36	253 51 43	ns ns ns
t_{PHL}	Maximum Propagation Delay A, B or C to any Y Output		2.0V 4.5V 6.0V	120 24 20	240 48 41		302 60 51	358 72 61	ns ns ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		2.0V 4.5V 6.0V	65 13 11	130 26 22		164 33 28	194 39 33	ns ns ns
t_{PLH}	Maximum Propagation Delay G1 to Output		2.0V 4.5V 6.0V	75 15 13	150 30 26		189 38 32	224 45 38	ns ns ns
t_{PHL}	Maximum Propagation Delay G1 to Output		2.0V 4.5V 6.0V	98 20 17	195 39 33		246 49 42	291 58 49	ns ns ns
t_{PLH}	Maximum Propagation Delay GL to Output		2.0V 4.5V 6.0V	88 18 15	175 35 30		221 44 37	261 52 44	ns ns ns
t_{PHL}	Maximum Propagation Delay GL to Output		2.0V 4.5V 6.0V	125 25 21	250 50 43		315 63 54	373 75 63	ns ns ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$, to any Y Output		2.0V 4.5V 6.0V	98 20 17	195 39 33		246 49 42	291 58 49	ns ns ns
t_S	Minimum Setup Time at A, B and C inputs		2.0V 4.5V 6.0V		100 20 17		125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time at A, B and C inputs		2.0V 4.5V 6.0V		50 10 8		63 13 11	75 15 13	ns ns ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13		95 19 16	110 22 19	ns ns ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		2.0V 4.5V 6.0V		80 16 14		100 20 18	120 24 21	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)			75					pF
C_{IN}	Maximum Input Capacitance			5	10		10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

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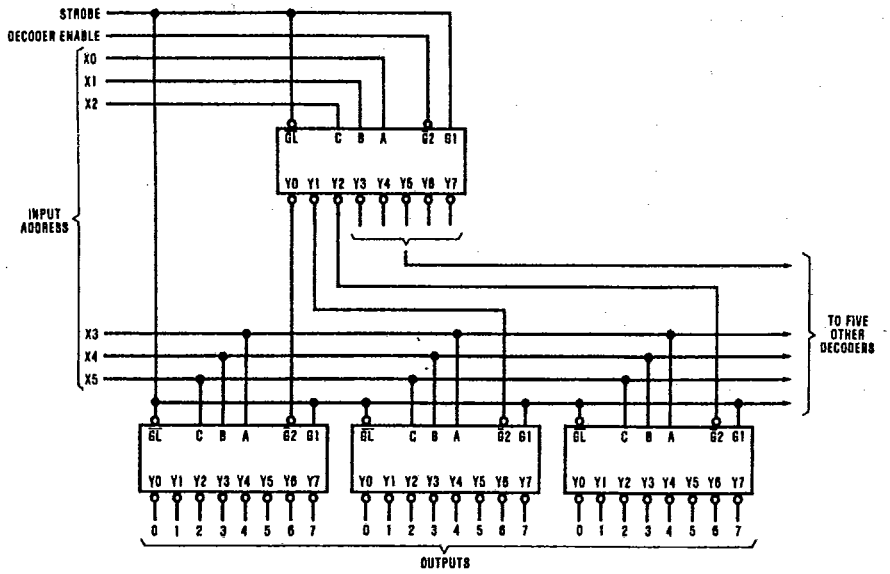
Typical Application



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6-Line to 64-Line Decoder with Input Address Storage

Truth Table

Inputs						Outputs							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address L; all others, H							

H = high level, L = low level, X = irrelevant