20-OUTPUT CLOCK DRIVER SC3506

FEATURES

- **20 clock outputs:**
  - Grouped into banks of 5 or 10 outputs
  - Output frequency of each bank is user selectable
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 65–75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **52-pin PQFP package**

APPLICATIONS

- **Compatible with Intel's Pentium™ processor**
- **Compatible with PowerPC™ processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**
- **Datacom and Telecom networks**

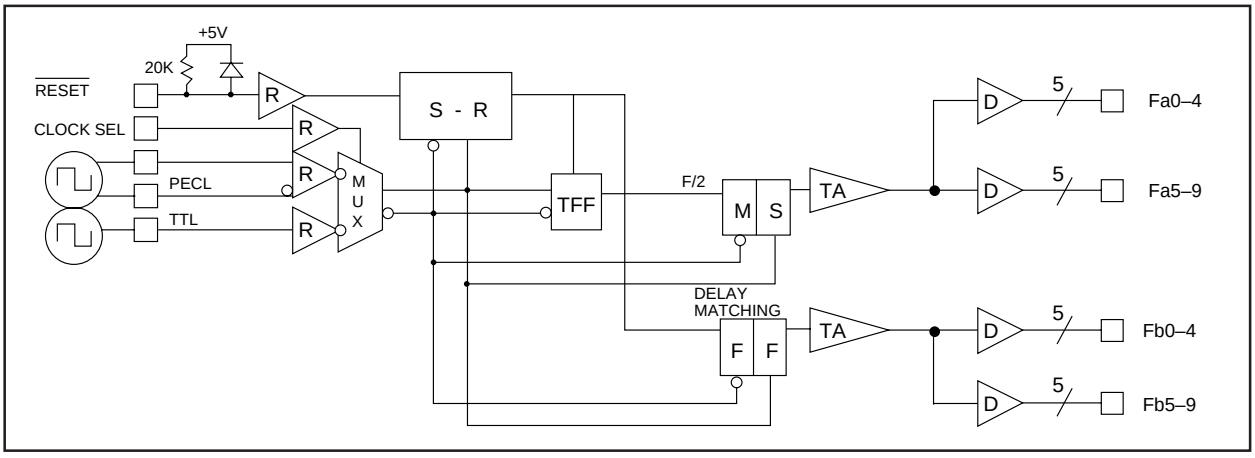
GENERAL DESCRIPTION

The SC3506 is a precision clock fan out drivers. It accepts a reference dock input from either a single-ended TTL source or a differential PECL frequency source. This reference clock input is distributed through dividers and buffers to the output clock drivers.

The 20 outputs are divided into groups of 5 or 10 outputs. The output frequency of each group can be F, F/2, F/4, or F/8, and is user selectable. Each of the clock driver products offers different combinations of divide ratios.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

SC3506 Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

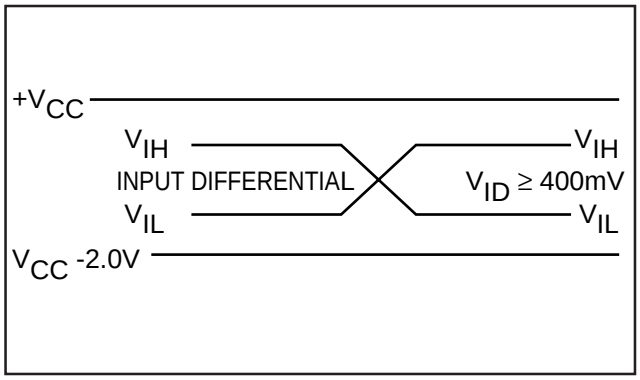
Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C (reference "AC Test/Evaluation Circuit")

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL, CSEL, BSEL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		50	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL, CSEL, BSEL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	70°C, Typ Pwr=350 mW		600	mW

1. Maximum test duration, one second.
2. The SC3506 features source series termination of approximately 40 Ohms to assist in matching 65–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The outputs have been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the outputs will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

Applied Micro Circuits Corporation
6290 Sequence Dr., San Diego, CA 92121-4358

AC Specifications—Using "AC Test/Evaluation Circuit"

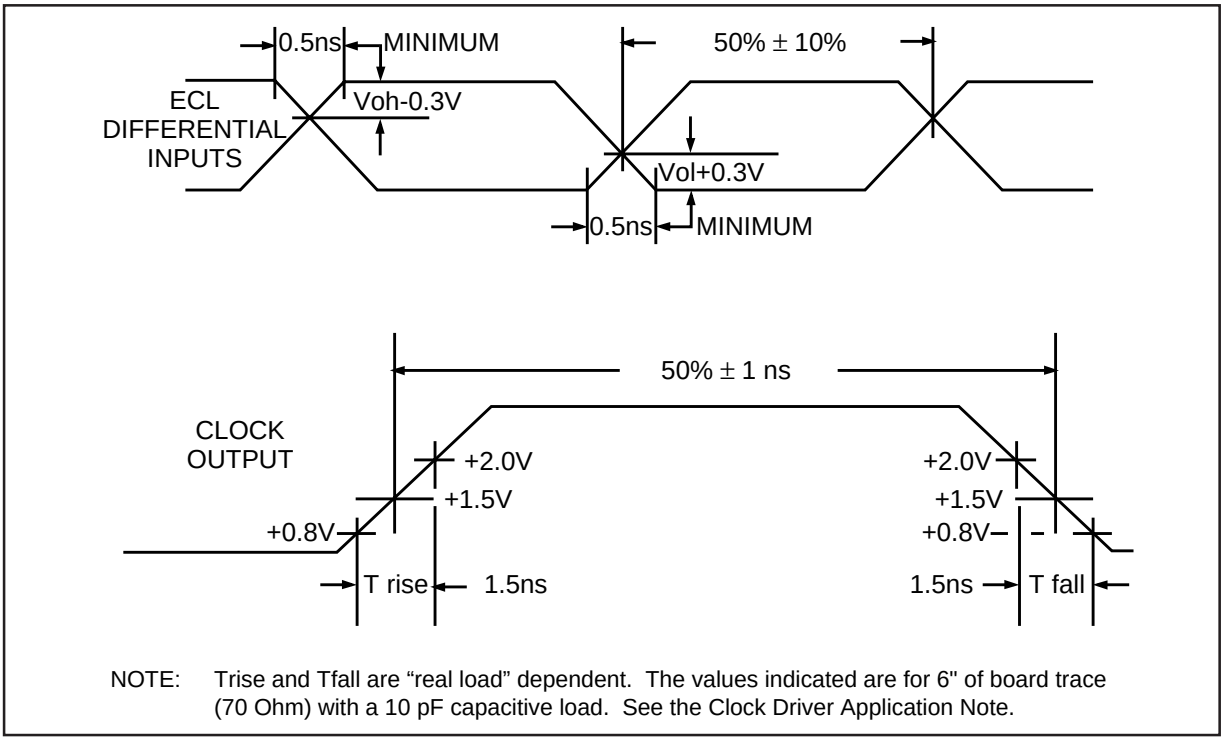
V_{CC} = +5.0V ± 5%, Ta = 0°C to +70°C, C_{LOAD} = 10pF

Parameter	SC3506	Units
Maximum Skew Across All Outputs Options: Standard –1 –2	 1.0 0.5 0.5	ns
Maximum Skew Chip to Chip Options: Standard –1 –2	 — — 1.0	
Maximum Skew within an Output Group	0.25	ns
Maximum Output Duty Cycle Asymmetry	±1.0	ns
Maximum TTL Input Frequency	80	MHz
Maximum PECL Differential Input Frequency	80	MHz
Maximum Rising/Falling Edge Rate	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be effected by voltage, temperature, and load (including the length of the PC trace). Only applies to divided outputs.
3. Typical skew derating factor for different loads is 50 ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pf capacitive load. See "AC Test/Evaluation Circuit." Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization.

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

DESCRIPTION OF OPERATION (Refer to Logic Diagrams)

AMCC has developed a single-chip clock shape and 20-output fan-out device using AMCC's advanced BiCMOS process. This design has been optimized for clock symmetry and absolute minimum skew across all twenty outputs.

For highest performance this approach requires a clock source input from a crystal-controlled oscillator (XCO) located adjacent to this clock driver. This oscillator, operating between +5V and ground, can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a divide-down counter and master-slave flip-flops for synchronization (refer to the Logic Diagrams).

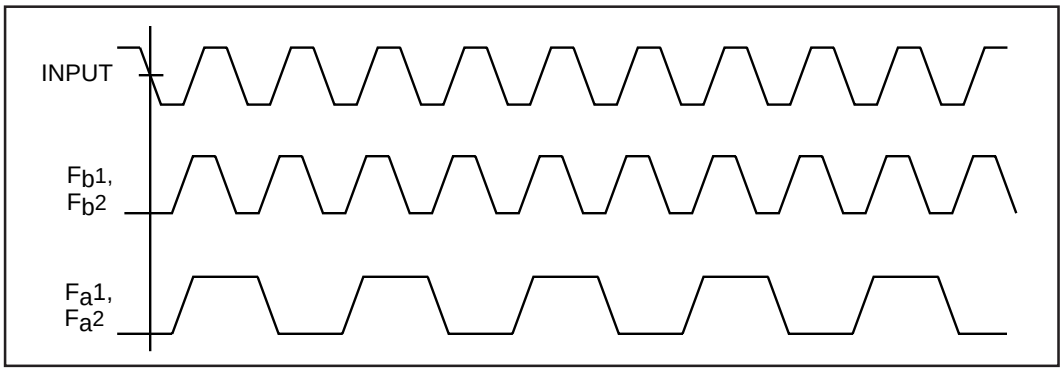
The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following five falling edge clock inputs (four clock inputs for the SC3506). At the expiration of RESET (high) outputs will resume, after five falling edge clock inputs (four clock inputs for the SC3506), from a high (leading edge) count origin (see Figure 5, Reset To Output Timing in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 65–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current.

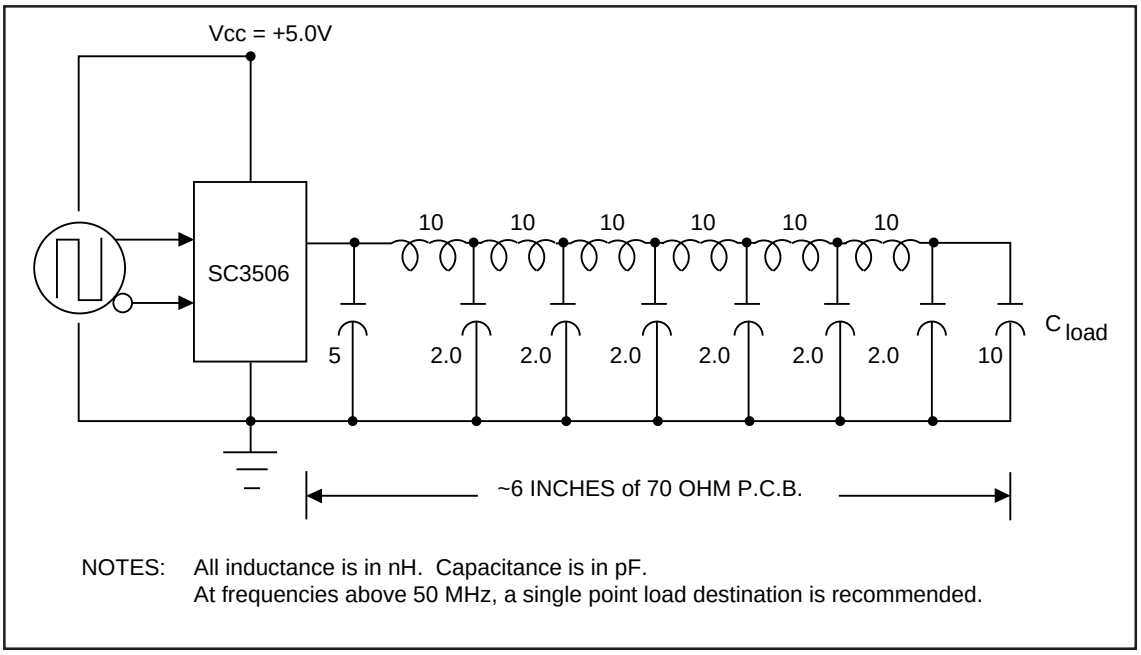
Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the clock driver will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

SC3506 Relative Output Timing



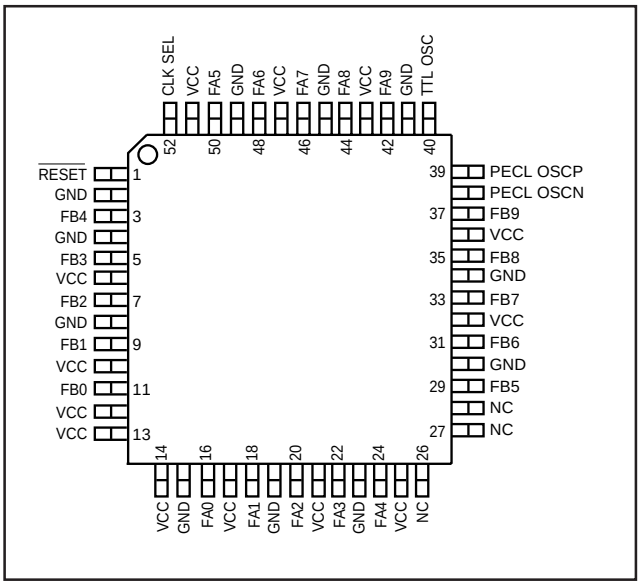
AC Test/Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

SC3506 has no frequency selection capabilities.

SC3506 Pinout



Power Management

The overall goal of managing the power dissipated by the clock driver is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the clock driver is determined by the load that each output drives and the frequency that each output is running. The "Output Power Dissipation" table summarizes these dependencies (see the "AC Test/Evaluation Circuit", for complete load definition).

The output power must be added to the core power (600 mW) of the clock driver to determine the total power being dissipated by the clock driver. This total power is then multiplied by the clock driver's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3506. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the clock driver is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an clock driver with 8 Fa outputs driving 10 pF loads at 66 MHz, 3 Fb outputs driving 5 pF loads at 33 MHz and 2 Fc outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

Core Power (SC3500)	= 600 mW
8 Fa, 10 pF, 66 MHz = (8 x 47 mW)	= 376 mW
2 Fa, no load, 66 MHz = (2 x 16 mW)	= 32 mW
3 Fb, 5 pF, 33 MHz = (3 x 19 mW)	= 57 mW
2 Fb, no load, 33 MHz = (2 x 12 mW)	= 24 mW
2 Fc, 15 pF, 33 MHz = (2 x 24 mW)	= 48 mW
3 Fc, no load, 33 MHz = (3 x 12 mW)	= 36 mW
Total Power	= 1173 mW

The design specifies a 70˚C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2˚C/watt. The clock driver's junction temperature would then be:

70˚C + (1.173 watts x 46.2˚C/watt) = 124˚C

Note this is below the 140˚C maximum junction temperature.

Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

SC3506 Product Selection Guide

	Output Frequency with Respect to Input Frequency					
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Number of Outputs ÷ 2 or 4	Special Features	Package
SC3506	20	10	10	N/A	—	52 PQFP

Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC3506 **Q** **– 1** **/TD**

Optional Shipping Configuration
Blank = 84-unit matrix tray
/D = dry pack
/TD = tape, reel and dry pack

Skew Option
Blank = 1.0 ns output-output skew
– 1 = 500 ps output-output skew
– 2 = 1.0 ns chip-to-chip skew

Package Option
Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC3506Q–1/D
52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.

Part Number	Standard	–1	–2
SC3506	✔	✔	✔

Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121
Phone: (619) 450-9333 • (800) 755-2622 • Fax: (619) 450-9885
http://www.amcc.com

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