



54VHC/74VHC157 Quad 2-Input Multiplexer

General Description

The VHC157 is an advanced high speed CMOS Quad 2-Channel Multiplexer fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select and enable inputs.

When the $\overline{\text{ENABLE}}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level.

The SELECT decoding determines whether the I_{0x} or I_{1x} inputs get routed to their corresponding outputs.

An Input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

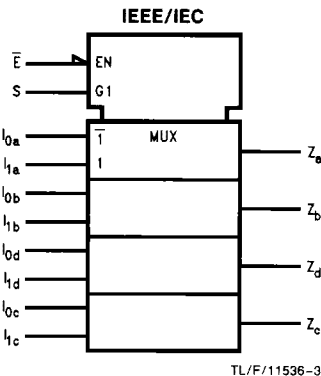
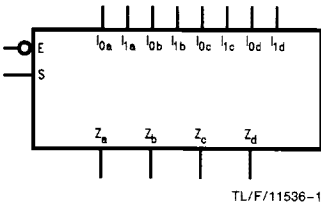
MILITARY SPECIFICATIONS ARE PRELIMINARY

Features

- High speed: $t_{PD} = 4.1 \text{ ns (typ.)}$ at $V_{CC} = 5V$
- Low power dissipation:
 $I_{CC} = 4 \mu\text{A (max.)}$ at $T_A = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min.)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: $V_{CC} \text{ (opr)} = 2V \sim 5.5V$
- Low noise: $V_{OLP} = 0.8V$ (max.)
- Pin and function compatible with 74HC157

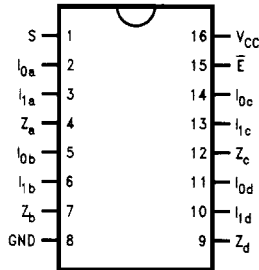
Ordering Code: See Section 5

Logic Symbols

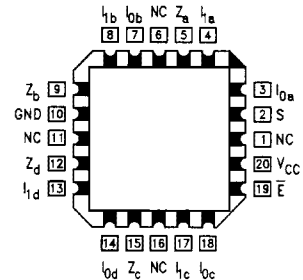


Connection Diagrams

Pin Assignment for DIP, Flatpack, SSOP and SOIC



Pin Assignment for LCC



Pin Names	Description
$I_{0a}-I_{0d}$	Source 0 Data Inputs
$I_{1a}-I_{1d}$	Source 1 Data Inputs
$\overline{\text{E}}$	Enable Input
S	Select Input
Z_a-Z_d	Outputs

Functional Description

The VHC157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The VHC157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the VHC157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The VHC157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

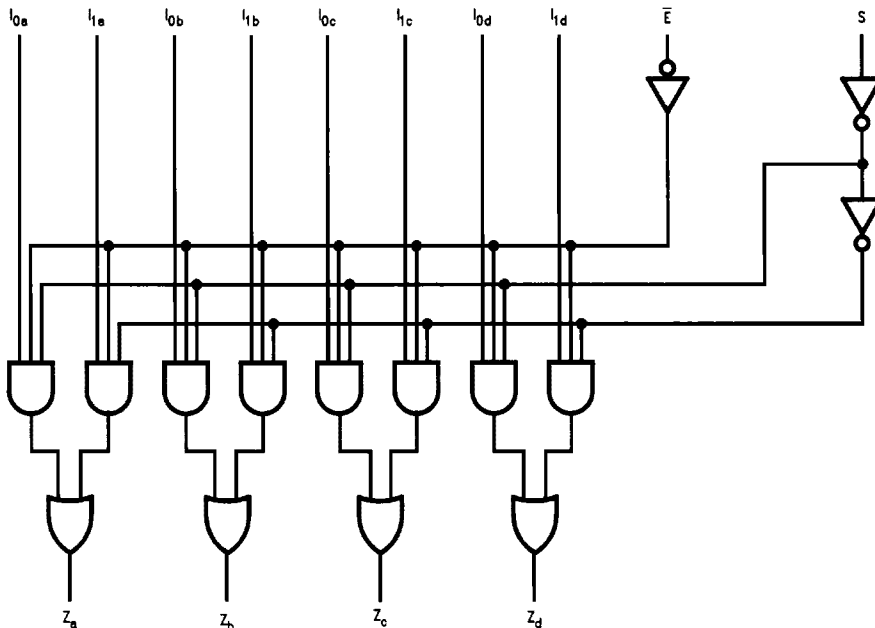
Inputs				Outputs
\bar{E}	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



TL/F/11536-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-0.5V to +7.0V
DC Output Voltage (V_{OUT})	-0.5V to $V_{CC} + 0.5V$
Input Diode Current (I_{IK})	-20 mA
Output Diode Current (I_{OK})	± 20 mA
DC Output Current (I_{OUT})	± 25 mA
DC V_{CC} /GND Current (I_{CC})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	
54 VHC	-55°C to +125°C
74 VHC	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 3.3V \pm 0.3V$	0 ~ 100 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC			54VHC		74VHC		Units	Conditions	
			$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C}$ to +125°C		$T_A = -40^\circ\text{C}$ to +85°C				
			Min	Typ	Max	Min	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0-5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0-5.5	0.50 0.3 V_{CC}			0.50 0.3 V_{CC}		0.50 0.3 V_{CC}		V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.0 2.9 3.0 4.4 4.5			1.9 2.9 4.4		1.9 2.9 4.4		V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu\text{A}$
		3.0 4.5	2.58 3.94			3.70		2.48 3.80		V		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5	0.0 0.1 0.0 0.1 0.0 0.1			0.1 0.1 0.1		0.1 0.1 0.1		V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu\text{A}$
		3.0 4.5	0.36 0.36			0.50 0.50		0.44 0.44		V		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$
I_{IN}	Input Leakage Current	0-5.5	± 0.1			± 1.0		± 1.0		μA	$V_{IN} = 5.5V$ or GND	
I_{CC}	Quiescent Supply Current	5.5	4.0					40.0		μA	$V_{IN} = V_{CC}$ or GND	

DC Characteristics for 'VHC Family Devices: See Section 2 for Waveforms (Continued)

Symbol	Parameter	V _{CC} (V)	74VHC		54VHC	74VHC		Units	Conditions	Fig. No.
			T _A = 25°C		T _A = -55°C to +125°C	T _A = -40°C to +85°C				
			Typ	Limits	Limits	Limits				
**V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	0.3	0.8				V	C _L = 50 pF	2-11, 12
**V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.3	-0.8				V	C _L = 50 pF	2-11, 12
**V _{IHD}	Minimum High Level Dynamic Input Voltage	5.0		3.5				V	C _L = 50 pF	2-11, 12
**V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		1.5				V	C _L = 50 pF	2-11, 12

**Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} (V)	74VHC			54VHC		74VHC		Units	Conditions	Fig. No.
			T _A = 25°C			T _A = -55°C to +125°C		T _A = -40°C to +85°C				
			Min	Typ	Max	Min	Max	Min	Max			
t _{PLH} , t _{PHL}	Propagation Delay I _n to Z _n	3.3 ± 0.3	6.2	9.7			1.0	11.5	ns	C _L = 15 pF	2-5	
			8.7	13.2			1.0	15.0		C _L = 50 pF	2-5	
		5.0 ± 0.5	4.1	6.4			1.0	7.5	ns	C _L = 15 pF	2-5	
			5.6	8.4			1.0	9.5		C _L = 50 pF	2-5	
t _{PLH} , t _{PHL}	Propagation Delay S to Z _n	3.3 ± 0.3	8.4	13.2			1.0	15.5	ns	C _L = 15 pF	2-6	
			10.9	16.7			1.0	19.0		C _L = 50 pF	2-6	
		5.0 ± 0.5	5.3	8.1			1.0	9.5	ns	C _L = 15 pF	2-6	
			6.8	10.1			1.0	11.5		C _L = 50 pF	2-6	
t _{PLH} , t _{PHL}	Propagation Delay E to Z _n	3.3 ± 0.3	8.7	13.6			1.0	16.0	ns	C _L = 15 pF	2-6	
			11.2	17.1			1.0	19.5		C _L = 50 pF	2-6	
		5.0 ± 0.5	5.6	8.6			1.0	10.0	ns	C _L = 15 pF	2-6	
			7.1	10.6			1.0	12.0		C _L = 50 pF	2-6	
C _{IN}	Input Capacitance		4	10			10	pF	V _{CC} = Open			
C _{PD}	Power Dissipation Capacitance		20					pF	(Note 1)			

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC (opr.)} = C_{PD} * V_{CC} * f_{IN} + I_{CC}.