



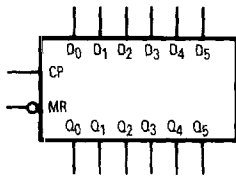
# Product Preview

## Hex D Flip-Flop with Master Reset

The MC74AC174/74ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

- Outputs Source/Sink 24 mA
- 'ACT174 Has TTL Compatible Inputs

### LOGIC SYMBOL



### PIN NAMES

- D<sub>0</sub>-D<sub>5</sub> Data Inputs
- CP Clock Pulse Input
- MR Master Reset Input
- Q<sub>0</sub>-Q<sub>5</sub> Outputs

### TRUTH TABLE

Inputs			Output
MR	CP	D	Q
L	X	X	L
H	↗	H	H
H	↗	L	L
H	L	X	Q

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- ↗ = LOW-to-HIGH Transition of Clock

**MC74AC174**  
**MC74ACT174**

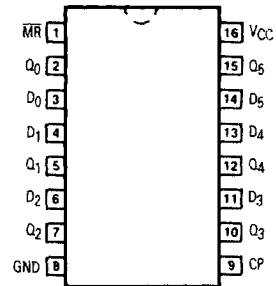
**HEX D FLIP-FLOP**  
**WITH MASTER RESET**



**N SUFFIX**  
**CASE 648-08**  
**PLASTIC**



**D SUFFIX**  
**CASE 751B-03**  
**PLASTIC**



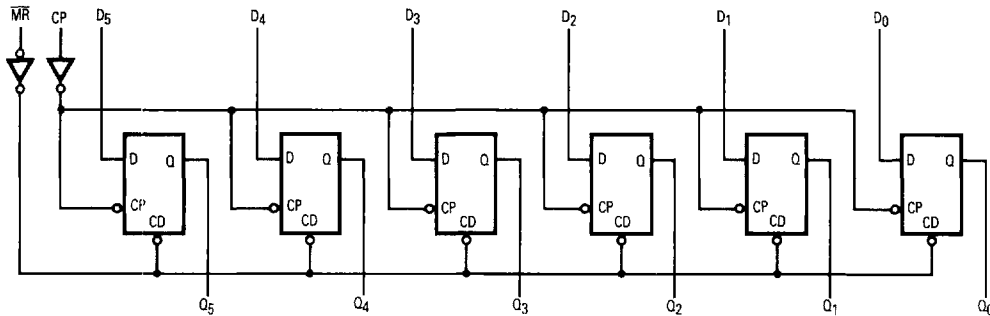
## MC74AC174 • MC74ACT174

### FUNCTIONAL DESCRIPTION

The MC74AC174/74ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ( $\overline{MR}$ ) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the

Master Reset ( $\overline{MR}$ ) will force all outputs LOW independent of Clock or Data inputs. The MC74AC174/74ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

### LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
$I_{CC}$	Maximum Quiescent Supply Current	80	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$ , $T_A = \text{Worst Case}$
$I_{CC}$	Maximum Quiescent Supply Current	8.0	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$ , $T_A = 25^\circ C$
$I_{CCT}$	Maximum Additional $I_{CC}$ /Input ('ACT174)	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$ , $V_{CC} = 5.5 V$ , $T_A = \text{Worst Case}$

**MC74AC174 • MC74ACT174**

**AC CHARACTERISTICS** (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC			74AC		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	90 100	100 125		70 100		MHz	3-3
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	3.3 5.0	1.0 1.0	9.0 6.0	11.5 8.5	1.0 1.0	12.5 9.5	ns	3-6
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	3.3 5.0	1.0 1.0	8.5 6.0	11 8.0	1.0 1.0	12 9.0	ns	3-6
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	3.3 5.0	1.0 1.0	9.0 7.0	11.5 9.0	1.0 1.0	12.5 10.5	ns	3-6

\*Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

**AC OPERATING REQUIREMENTS**

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC		74AC		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum				
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	2.5 2.0	6.5 5.0	7.0 5.5		ns	3-9
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	1.0 0.5	3.0 3.0	3.0 3.0		ns	3-9
t <sub>w</sub>	MR Pulse Width, LOW	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0		ns	3-6
t <sub>w</sub>	CP Pulse Width	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0		ns	3-6
t <sub>rec</sub>	Recovery Time MR to CP	3.3 5.0	0 0	2.5 2.0	2.5 2.0		ns	3-6

\*Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

**MC74AC174 • MC74ACT174**

**AC CHARACTERISTICS** (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT			74ACT		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	165	200		140		MHz	3-3
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-6
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-6
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	5.0	1.0	6.5	9.5	1.0	11	ns	3-6

\*Voltage Range 5.0 is 5.0 V ± 0.5 V

**AC OPERATING REQUIREMENTS**

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT		74ACT		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum				
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	0.5	1.5	1.5	ns	3-9	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	1.0	2.0	2.0	ns	3-9	
t <sub>w</sub>	MR Pulse Width, LOW	5.0	1.5	3.0	3.5	ns	3-6	
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	1.5	3.0	3.5	ns	3-6	
t <sub>rec</sub>	Recovery Time MR to CP	5.0	-1.0	0.5	0.5	ns	3-6	

\*Voltage Range 5.0 is 5.0 V ± 0.5 V

**CAPACITANCE**

Symbol	Parameter	Value Typ	Units	Test Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0 V
C <sub>PD</sub>	Power Dissipation Capacitance	85	pF	V <sub>CC</sub> = 5.0 V