

AC825 • ACT825 • AC826 • ACT826

NATIONAL SEMICONDUCTOR LOGIC D E D 6501122 0062708 0

54AC/74AC825 • 54ACT/74ACT825 54AC/74AC826 • 54ACT/74ACT826

T-46-07-11

8-Bit D-Type Flip-Flop

Description

The 'AC'/ACT825 and 'AC'/ACT826 are 8-bit buffered registers. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface.

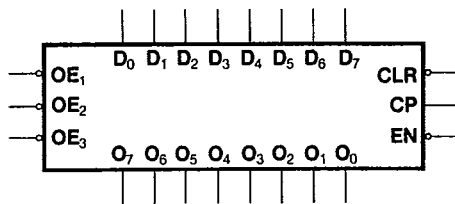
The 'AC'/ACT825 has noninverting outputs; the 'AC'/ACT826 has inverting outputs.

The 'AC'/ACT825 is fully compatible with AMD's AM29825.

- Outputs Source/Sink 24 mA
- Inputs and Outputs are on Opposite Sides
- 'ACT825 and 'ACT826 have TTL-Compatible Inputs

Ordering Code: See Section 6

Logic Symbol ('AC'/ACT825)*

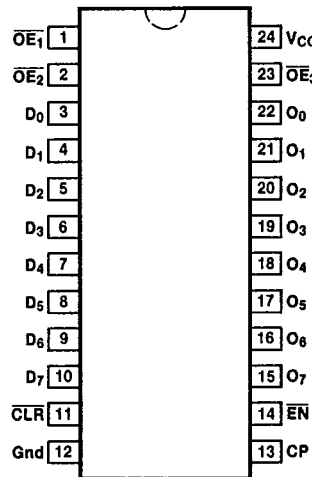


*The 'AC'/ACT826 has inverting outputs.

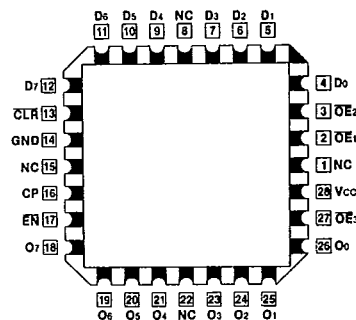
Pin Names

D ₀ - D ₇	Data Inputs
O ₀ - O ₇	Data Outputs ('AC'/ACT825)
\bar{O}_0 - \bar{O}_7	Data Outputs ('AC'/ACT826)
\bar{OE}_1 , \bar{OE}_2 , \bar{OE}_3	Output Enables
\bar{EN}	Clock Enable
\bar{CLR}	Clear
CP	Clock Input

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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Functional Description

The 'AC/ACT825 and 'AC/ACT826 consist of eight D-type edge-triggered flip-flops. These devices have 3-state outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With \overline{OE}_1 , \overline{OE}_2 and \overline{OE}_3 LOW, the contents of the flip-flops are available at the outputs. When one of \overline{OE}_1 , \overline{OE}_2 or \overline{OE}_3 is HIGH, the outputs go to the high impedance state.

Operation of the \overline{OE} input does not affect the state of the flip-flops. The 'AC/ACT825 and 'AC/ACT826 have Clear (\overline{CLR}) and Clock Enable (\overline{EN}) pins. These pins are ideal for parity bus interfacing in high performance systems.

When \overline{CLR} is LOW and \overline{OE} is LOW, the outputs are LOW. When \overline{CLR} is HIGH, data can be entered into the flip-flops. When \overline{EN} is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When \overline{EN} is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Outputs		Function
\overline{OE}	\overline{CLR}	\overline{EN}	CP	Dn	Q	O ('825)	\overline{O} ('826)	
H	X	L	\downarrow	L	L	Z	Z	High Z
H	X	L	\downarrow	H	H	Z	Z	High Z
H	L	X	X	X	L	Z	Z	Clear
L	L	X	X	X	L	L	L	Clear
H	H	H	X	X	NC	Z	Z	Hold
L	H	H	X	X	NC	NC	NC	Hold
H	H	L	\downarrow	L	L	Z	Z	Load
H	H	L	\downarrow	H	H	Z	Z	Load
L	H	L	\downarrow	L	L	L	H	Load
L	H	L	\downarrow	H	H	H	L	Load

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 \downarrow = LOW-to-HIGH Transition
 NC = No Change

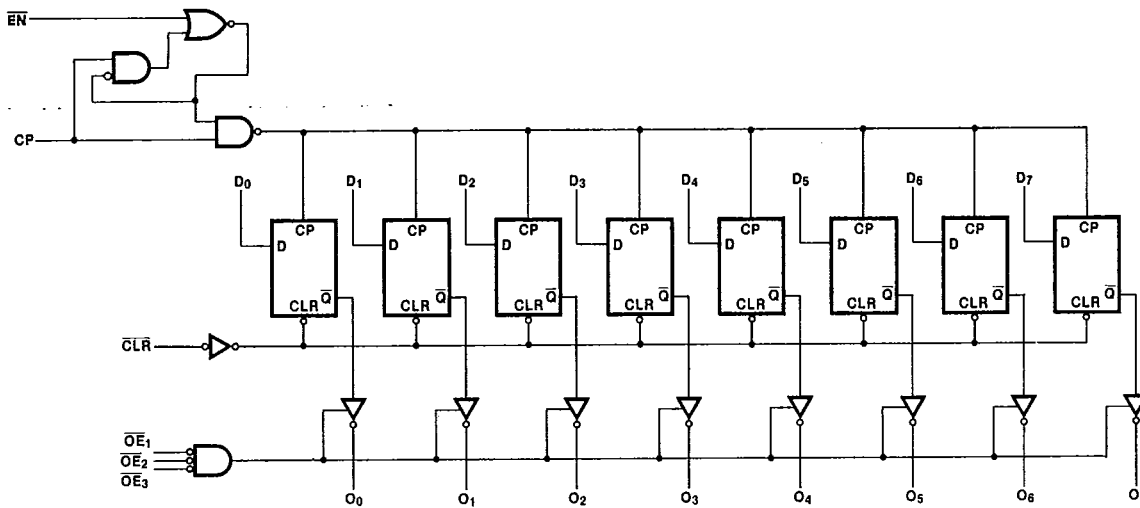
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Logic Diagram ('AC/ACT825)

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/ACT826 also has the same logic diagram with inverting outputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$, $T_A = \text{Worst Case}$
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$, $T_A = 25^\circ C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT825/826)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$ $V_{CC} = 5.5 V$, $T_A = \text{Worst Case}$

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	100						MHz	3-3	
t _{PLH}	Propagation Delay CP to O _n	3.3 5.0	9.0						ns	3-6	
t _{PHL}	Propagation Delay CP to O _n	3.3 5.0	9.0 6.5						ns	3-6	
t _{PHL}	Propagation Delay CLR to O _n	3.3 5.0	14.5 10.5						ns	3-6	
t _{PZH}	Output Enable Time OE to O _n	3.3 5.0	9.0 6.0						ns	3-7	
t _{PZL}	Output Enable Time OE to O _n	3.3 5.0	9.5 6.5						ns	3-8	
t _{PHZ}	Output Disable Time OE to O _n	3.3 5.0	12.5 8.5						ns	3-7	
t _{PLZ}	Output Disable Time OE to O _n	3.3 5.0	12.0 7.5						ns	3-8	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74AC	54AC	74AC	Units	Fig. No.
			TA = +25°C CL = 50 pF	TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum			
ts	Setup Time, HIGH or LOW Dn to CP	3.3	3.0			ns	3-9
		5.0	2.0				
th	Hold Time, HIGH or LOW Dn to CP	3.3	2.0			ns	3-9
		5.0	1.5				
ts	Setup Time, HIGH or LOW EN to CP	3.3	3.0			ns	3-9
		5.0	2.0				
th	Hold Time, HIGH or LOW EN to CP	3.3	2.0			ns	3-9
		5.0	1.5				
tw	CP Pulse Width HIGH or LOW	3.3	3.5			ns	3-6
		5.0	2.5				
tw	CLR Pulse Width, LOW	3.3	5.0			ns	3-6
		5.0	3.5				
trec	CLR to CP Recovery Time	3.3	2.0			ns	3-9
		5.0	1.5				

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

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Symbol	Parameter	V _{cc} * (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	110						MHz	3-3	
t _{PLH}	Propagation Delay CP to O _n	5.0	8.0						ns	3-6	
t _{PHL}	Propagation Delay CP to O _n	5.0	8.0						ns	3-6	
t _{PHL}	Propagation Delay CLR to O _n	5.0	12.0						ns	3-6	
t _{PZH}	Output Enable Time OE to O _n	5.0	7.5						ns	3-7	
t _{PZL}	Output Enable Time OE to O _n	5.0	8.0						ns	3-8	
t _{PHZ}	Output Disable Time OE to O _n	5.0	11.0						ns	3-7	
t _{PLZ}	Output Disable Time OE to O _n	5.0	9.5						ns	3-8	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74ACT	54ACT	74ACT	Units	Fig. No.
			TA = +25°C CL = 50 pF	TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum			
ts	Setup Time, HIGH or LOW Dn to CP	5.0	2.0			ns	3-9
th	Hold Time, HIGH or LOW Dn to CP	5.0	1.0			ns	3-9
ts	Setup Time, HIGH or LOW EN to CP	5.0	2.0			ns	3-9
th	Hold Time, HIGH or LOW EN to CP	5.0	1.5			ns	3-9
tw	CP Pulse Width HIGH or LOW	5.0	3.0			ns	3-6
tw	CLR Pulse Width, LOW	5.0	3.5			ns	3-6
trec	CLR to CP Recovery Time	5.0	1.5			ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance		pF	Vcc = 5.5 V