

December 1997

## Fast CMOS 16-Bit Registered Transceiver

### Features

- Advanced 0.6 micron CMOS Technology
- 5V Tolerant Inputs and Outputs
- Supports Live Insertion of PCBs
- 2.0V to 3.6V  $V_{CC}$  Supply Range
- Balanced 24mA Output Drive
- Low Ground Bounce Outputs
- ESD Protection Exceeds 2000V, HBM; 200V, MM
- Functionally Compatible with FCT3, LVC, LVT, and 74 Series Logic Families

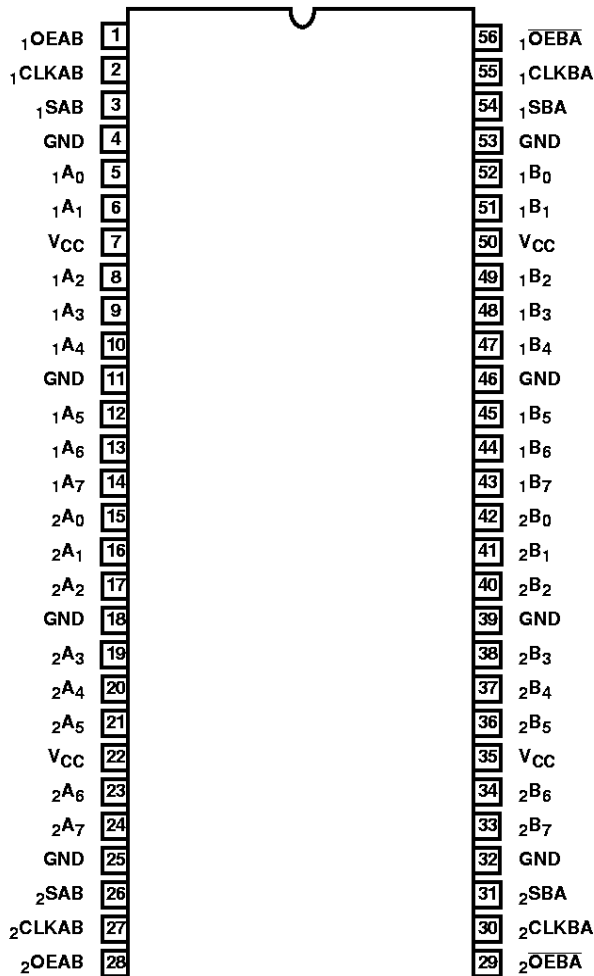
### Description

The CD74LCX16652 is a 16-bit registered transceiver organized as two independent 8-bit bus transceivers. It is designed with Three-State D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable controls ( $\chi_{OEAB}$  and  $\chi_{OEBA}$ ) to control the transceiver functions. The Select ( $\chi_{SAB}$  and  $\chi_{SBA}$ ) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74LCX16652 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

### Pinout

CD74LCX16652 (SSOP, TSSOP)  
TOP VIEW

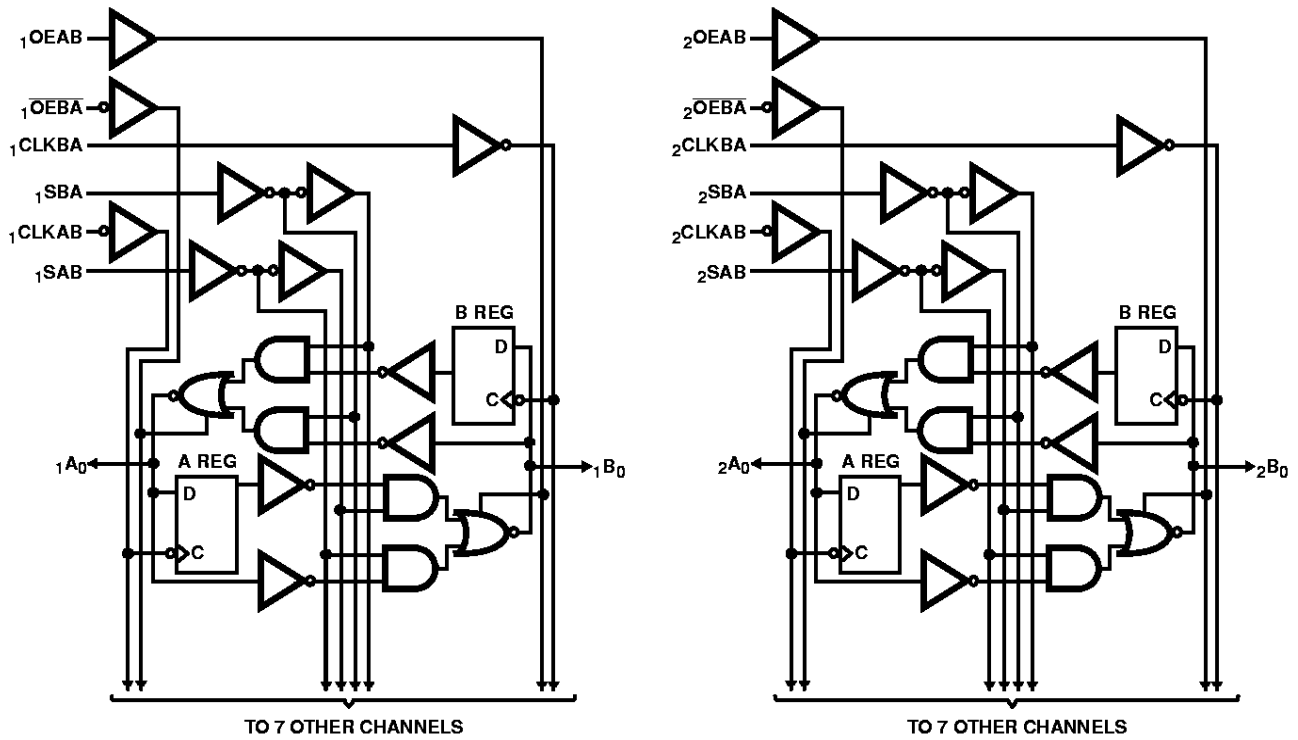


### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LCX16652MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LCX16652SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

**Functional Block Diagram**

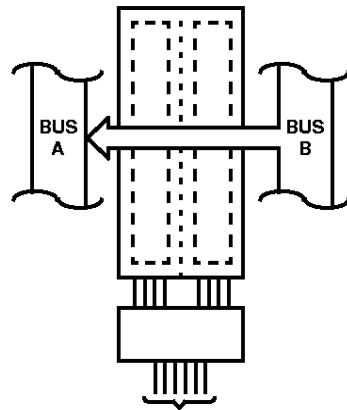


TRUTH TABLE (NOTE 1)

FUNCTION/OPERATION	INPUTS						DATA I/O	
	xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified (Note 2)
Store A in Both Registers	H	H	↑	↑	X (Note 3)	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified (Note 2)	Input
Store B in Both Registers	L	L	↑	↑	X	X (Note 3)	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

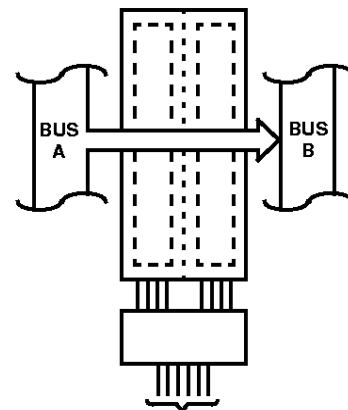
NOTES:

- H = High Voltage Level  
L = Low Voltage Level  
X = Don't Care  
↑ = LOW-to-HIGH transition
- The data output functions may be enabled or disabled by various signals at the xOEAB or xOEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.  
Select control = H: clocks must be staggered in order to load both registers.



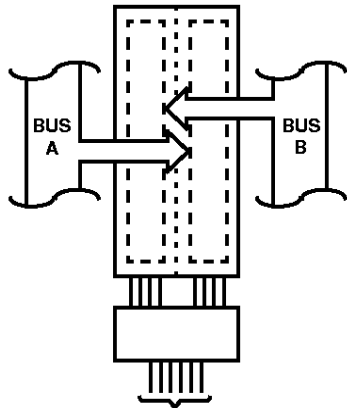
$\overline{xOEAB}$   $\overline{xOEBA}$   $xCLKAB$   $xCLKBA$   $xSAB$   $xSBA$   
 L L X X X L

FIGURE 1. REAL-TIME TRANSFER BUS B TO A



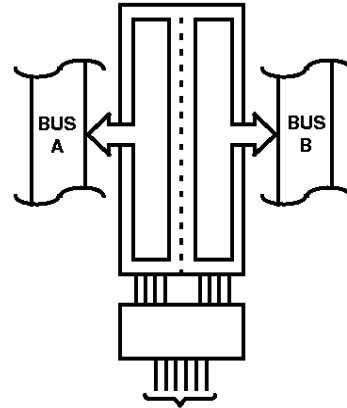
$\overline{xOEAB}$   $\overline{xOEBA}$   $xCLKAB$   $xCLKBA$   $xSAB$   $xSBA$   
 H H X X L X

FIGURE 2. REAL-TIME TRANSFER BUS A TO B



$\overline{xOEAB}$   $\overline{xOEBA}$   $xCLKAB$   $xCLKBA$   $xSAB$   $xSBA$   
 X H ↑ X X X  
 L X X ↑ X X  
 L H ↑ ↑ X X

FIGURE 3. STORAGE FROM A AND/OR B



$\overline{xOEAB}$   $\overline{xOEBA}$   $xCLKAB$   $xCLKBA$   $xSAB$   $xSBA$   
 H L H or L H or L H H

FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

**Pin Descriptions**

PIN NAME	DESCRIPTION
$x^A_x$	Data Register A Inputs Data Register B Outputs
$x^B_x$	Data Register B Inputs Data Register A Outputs
$xCLKAB, xCLKBA$	Clock Pulse Inputs
$xSAB, xSBA$	Output Data Source Select Inputs
$\overline{xOEAB}, \overline{xOEBA}$	Output Enable Inputs
GND	Ground
$V_{CC}$	Power

# CD74LCX16652

## Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V  
 DC Output Current ..... 120mA

## Operating Conditions

Temperature Range ..... -40°C to 85°C  
 Supply Voltage to Ground Potential  
   Inputs and V<sub>CC</sub> Only ..... -0.5V to 7.0V  
 Supply Voltage, V<sub>CC</sub>  
   Operating ..... 2.0V (Min), 3.6V (Max)  
   Data Retention ..... 1.5V (Min), 3.6V (Max)  
 Supply Voltage to Ground Potential  
   Outputs and D/O Only ..... -0.5V to 7.0V

## Thermal Information

Thermal Resistance (Typical, Note 4) θ<sub>JA</sub> (°C/W)  
   TSSOP Package ..... 85  
   SSOP Package ..... 70  
 Maximum Junction Temperature ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C  
   (Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

4. θ<sub>JA</sub> is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS	MIN	(NOTE 6) TYP	MAX	UNITS	
<b>DC ELECTRICAL SPECIFICATIONS</b> Over the Operating Range, T <sub>A</sub> = -40°C to 85°C, V <sub>CC</sub> = 2.7V to 3.6V							
Input HIGH Voltage	V <sub>IH</sub>	Guaranteed Logic HIGH Level	2.0	-	-	V	
Input LOW Voltage (Input and I/O Pins)	V <sub>IL</sub>	Guaranteed Logic LOW Level	-	-	0.8	V	
Output HIGH Voltage	V <sub>OH</sub>	V <sub>CC</sub> = 2.7V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	-	-	V
		V <sub>CC</sub> = 2.7V	I <sub>OH</sub> = -12mA	2.2	-	-	V
		V <sub>CC</sub> = 3.0V	I <sub>OH</sub> = -18mA	2.4	-	-	V
			I <sub>OH</sub> = -24mA	2.2	-	-	V
Output LOW Voltage	V <sub>OL</sub>	V <sub>CC</sub> = 2.7V to 3.6V	I <sub>OL</sub> = 0.1mA	-	-	0.2	V
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	-	-	0.4	V
		V <sub>CC</sub> = 3V	I <sub>OL</sub> = 16mA	-	-	0.4	V
			I <sub>OL</sub> = 24mA	-	-	0.55	V
Clamp Diode Voltage	V <sub>IK</sub>	V <sub>CC</sub> = Min, I <sub>IN</sub> = -18mA	-	-0.7	-1.2	V	
Input Current	I <sub>I</sub>	V <sub>CC</sub> = 2.7V to 3.6V	0 ≤ V <sub>I</sub> ≤ 5.5V	-	-	±5	μA
High Impedance Output Current (Three-State)	I <sub>OZ</sub>	V <sub>CC</sub> = 2.7V to 3.6V	0 ≤ V <sub>O</sub> ≤ 5.5V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	-	±5	μA
Power Down Disable	I <sub>OFF</sub>	V <sub>CC</sub> = 0V	V <sub>IN</sub> or V <sub>OUT</sub> ≤ 5.5V	-	-	10	μA
Quiescent Power Supply Current	I <sub>CC</sub>	V <sub>CC</sub> = Max	V <sub>IN</sub> = GND or V <sub>CC</sub>	-	0.1	10	μA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI <sub>CC</sub>	V <sub>CC</sub> = Max	V <sub>IN</sub> = V <sub>CC</sub> - 0.6V (Note 7)	-	-	500	μA
<b>CAPACITANCE</b>							
Input Capacitance (Note 8)	C <sub>IN</sub>	V <sub>CC</sub> = Open, V <sub>IN</sub> = 0V or V <sub>CC</sub>	-	7	-	pF	
Output Capacitance (Note 8)	C <sub>OUT</sub>	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = 0V or V <sub>CC</sub>	-	8	-	pF	
Power Dissipation Capacitance (Note 9)	C <sub>PD</sub>	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = 0V or V <sub>CC</sub> , f = 10MHz	-	20	-	pF	

## CD74LCX16652

### Switching Specifications Over Operating Range

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> = 3.3V ±0.3V		V <sub>CC</sub> = 2.7V		UNITS
			MIN	MAX	MIN	MAX	
Propagation Delay, Bus to Bus	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	1.5	5.7	1.5	6.2	ns
Output Enable Time, xOEAB or xOEBA to Bus	t <sub>PZL</sub> , t <sub>PZH</sub>		1.5	7.0	1.5	8.0	ns
Output Disable Time, xOEAB or xOEBA to Bus	t <sub>PHZ</sub> , t <sub>PLZ</sub>		1.5	6.5	1.5	7.0	ns
Propagation Delay, Clock to Bus	t <sub>PHL</sub> , t <sub>PLH</sub>		1.5	6.2	1.5	7.0	ns
Propagation Delay, .xSBA to sSAB to Bus	t <sub>PLH</sub> , t <sub>PHL</sub>		1.5	6.5	1.5	7.0	ns
Setup Time, HIGH or LOW, Bus to Clock	t <sub>SU</sub>		2.5	-	2.5	-	ns
Hold Time HIGH or LOW, Bus to Clock	t <sub>H</sub>		1.5	-	1.5	-	ns
Clock Pulse Width, HIGH or LOW (Note 12)	t <sub>W</sub>		3.0	-	3.0	-	ns
Output Skew (Note 13)	t <sub>SK(O)</sub>		-	1.0	-	-	ns

### Dynamic Switching Characteristics T<sub>A</sub> = 25°C

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	TYP	UNITS
Dynamic LOW Peak Voltage	V <sub>OLP</sub>	V <sub>CC</sub> = 3.3V, C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.8	V
Dynamic LOW Valley Voltage	V <sub>OLV</sub>	V <sub>CC</sub> = 3.3V, C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.8	V

#### NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V<sub>CC</sub> = 3.3V, 25°C ambient and maximum loading.
7. Per TTL driven input; all other inputs at V<sub>CC</sub> or GND.
8. This parameter is determined by device characterization but is not production tested.
9. C<sub>PD</sub> determines the no-load dynamic power consumption per latch. It is obtained by the following relationship:  
P<sub>D</sub> (total power per latch) = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> (C<sub>PD</sub> + C<sub>L</sub>) where f<sub>i</sub> = input frequency, C<sub>L</sub> = output load capacitance, V<sub>CC</sub> = supply range.
10. See test circuit and waveforms.
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. This parameter is guaranteed but not production tested.
13. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
14. Measured with n-1 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.