AUTO-ZEROED MONOLITHIC OPERATIONAL AMPLIFIER

FEATURES

- First Monolithic Chopper-Stabilized Amplifier With On-Chip Nulling Capacitors
- Offset Voltage ..... 5 μV
- Offset Voltage Drift ..... 0.05 μV/°C
- Low Supply Current ..... 350 μA
- High Common-Mode Rejection ..... 116 dB
- Single Supply Operation ..... 4.5V to 16V
- High Slew Rate ..... 2.5 V/μs
- Wide Bandwidth ..... 1.5 MHz
- High Open-Loop Voltage Gain (R_L = 10 kΩ) ..... 120 dB
- Low Input Voltage Noise (0.1 Hz to 1 Hz) ..... 0.65 μV_{P-P}
- Pin Compatible With ICL7650
- Lower System Parts Count

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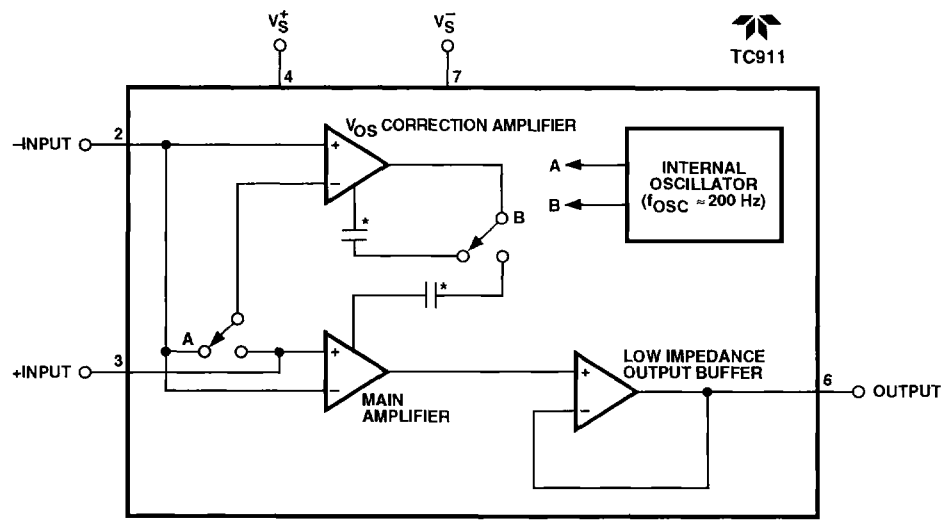
FUNCTIONAL DIAGRAM



*NOTE: Internal capacitors. No external capacitors required.

TC911

GENERAL DESCRIPTION

The TC911 CMOS auto-zeroed operational amplifier is the first complete monolithic chopper-stabilized amplifier. Chopper operational amplifiers like the ICL7650/7652 and LTC1052 require user-supplied, external offset compensation storage capacitors. **External capacitors are not required with the TC911.** Just as easy to use as the conventional 741 type amplifier, the TC911 significantly reduces offset voltage errors. Pinout matches the OP07/741/7650 8-pin mini-DIP configuration.

Several system benefits arise by eliminating the external chopper capacitors: lower system parts count; reduced assembly time and cost; greater system reliability; reduced PC board layout effort and greater board area utilization. Also, space savings can be significant in multiple-amplifier designs.

Electrical specifications include 15 μV maximum offset voltage, 0.15 μV/°C maximum offset voltage temperature coefficient. Offset voltage error is five times lower than the premium OP07E bipolar device. The TC911 improves offset drift performance by eight times.

Low offset voltage errors eliminate trim procedures during manufacturing, periodic recalibrations, and reliability problems caused by damaged or misadjusted trim potentiometers.

The TC911 automatically corrects offset voltage drift with time. Operational amplifier long-term drift is less easily controlled and more expensive to maintain when low offset errors are obtained by trimming thin-film resistors. The TC911 internal circuits correct errors repetitively at a 200 Hz rate. Long-term drift is effectively eliminated.

The TC911 operates from dual or single power supplies. Supply current is typically 350 μA. Single 4.5V to 16V supply operation is possible, making single 9V battery operation possible. The TC7660 DC-to-DC converter can easily supply a negative potential in dual-supply applications where only a +5V system supply is available.

Open-loop voltage gain is 115 dB minimum with a 10 kΩ load. Unity gain bandwidth is 1.5 MHz. Slew rate is 2.5 V/μs. Common-mode rejection ratio is 116 dB. Input common-mode range extends from 2V below the positive supply to the negative supply.

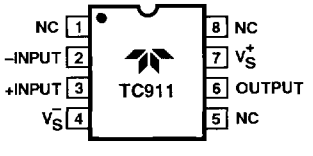
The TC911 is available in three package types: 8-pin plastic DIP, ceramic DIP and SO package. Die are available for hybrid applications.

For precision dual- and quad-monolithic chopper-stabilized amplifiers, see the TC913 (dual) and TC914 (quad) data sheets.

ORDERING INFORMATION

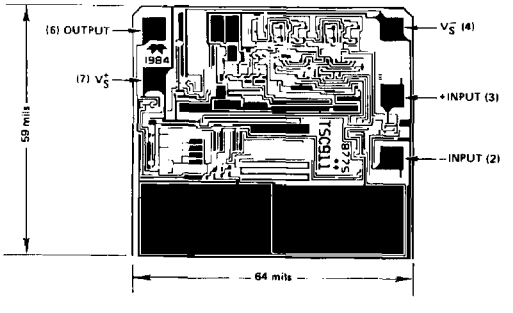
Part No.	Package	Temperature Range	Maximum Offset Voltage
TC911ACPA	8-Pin Plastic DIP	0°C to +70°C	15 μV
TC911ACOA	8-Pin SO	0°C to +70°C	15 μV
TC911BCPA	8-Pin Plastic DIP	0°C to +70°C	30 μV
TC911BCOA	8-Pin SO	0°C to +70°C	30 μV
TC911AIJA	8-Pin CerDIP	–25°C to +85°C	15 μV
TC911BIJA	8-Pin CerDIP	–25°C to +85°C	30 μV

PIN CONFIGURATION (SO and DIP)



NC = NO INTERNAL CONNECTION

BONDING DIAGRAM



NOTES: 1. Back of die is common to V_{CC}.
2. Back of die is not metalized.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) ..... +18V
Input Voltage ..... (V_S^++0.3V) to (V_S^- –0.3V)
Current into Any Pin ..... 10 mA
While Operating ..... 100 µA
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Operating Temperature Range
C Device ..... 0°C to +70°C
I Device ..... –25°C to +85°C

Package Power Dissipation (T_A = +25°C)
CerDIP ..... 500 mW
Plastic DIP and SO ..... 375 mW

Static-sensitive device. Unused devices should be stored in conductive material. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

ELECTRICAL CHARACTERISTICS: V_S = ±5V, T_A = +25°C, unless otherwise indicated.

			TC911A			TC911B			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage	T_A = +25°C	—	5	15	—	15	30	µV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ +70°C	—	0.05	0.15	—	0.1	0.25	µV/°C
		–25°C ≤ T_A ≤ +85°C	—	0.05	0.15	—	0.1	0.25	µV/°C
I_B	Average Input Bias Current	T_A = +25°C	—	—	70	—	—	120	pA
		0°C ≤ T_A ≤ +70°C	—	—	3	—	—	4	nA
		–25°C ≤ T_A ≤ +85°C	—	—	4	—	—	6	nA
I_{OS}	Average Input Offset Current		—	5	20	—	10	40	pA
e_N	Input Voltage Noise	0.1 to 1 Hz, R_S ≤ 100Ω	—	0.65	—	—	0.65	—	μV_{P-P}
		0.1 to 10 Hz, R_S ≤ 100Ω	—	11	—	—	11	—	μV_{P-P}
CMRR	Common-Mode Rejection Ratio	$V_S^- \le V_{CM} \le V_S^+ - 2.2$	110	116	—	105	110	—	dB
CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ –2	V_S^-	—	V_S^+ –2	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4V	115	120	—	110	120	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- +0.3	—	V_S^+ –0.9	V_S^- +0.3	—	V_S^+ –0.9	V
BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pF	—	2.5	—	—	2.5	—	V/µs
PSRR	Power Supply Rejection Ratio	±3.3V to ±5.5V	112	—	—	105	—	—	dB
V_S	Operating Supply Voltage Range	Split Supply	±3	—	±8	±3	—	±8	V
		Single Supply	4.5	—	16	4.5	—	16	V
I_S	Quiescent Supply Current	V_S = ±5V	—	350	600	—	—	800	µA

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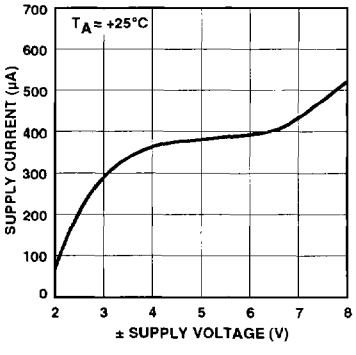
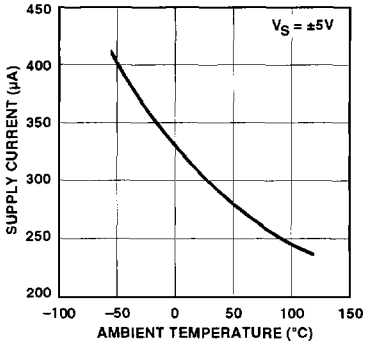
TC911

TYPICAL CHARACTERISTICS CURVES

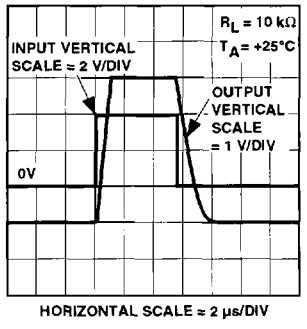
Supply Current vs ± Supply Voltage



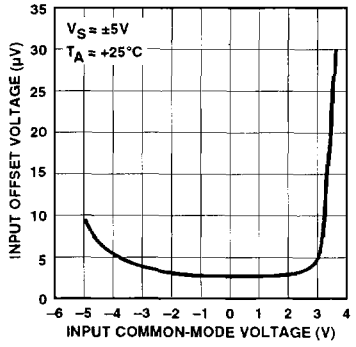
Supply Current vs Temperature



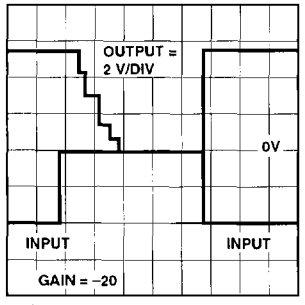
Large Signal Output Switching Waveform



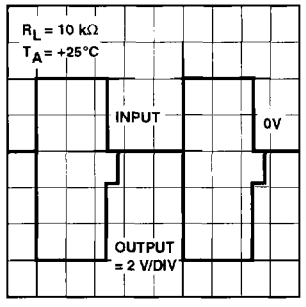
Input Offset Voltage vs Common-Mode Voltage



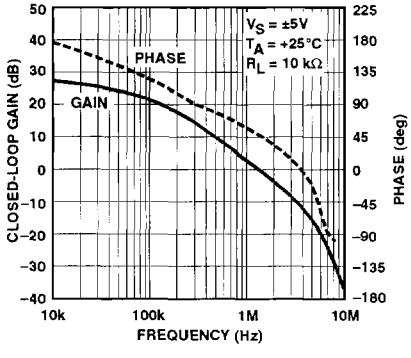
Positive Overload Recovery Time



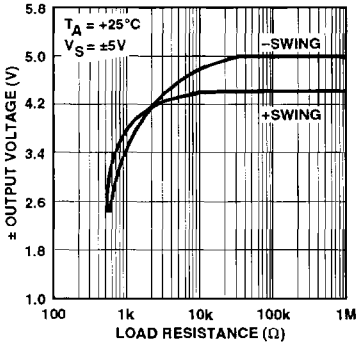
Negative Overload Recovery Time



Gain and Phase vs Frequency



Output Voltage Swing vs Load Resistance



Pin Compatibility

The CMOS TC911 is pin compatible with the GE/Intersil ICL7650 chopper-stabilized amplifier. The ICL7650 must use external 0.1 μF capacitors connected at pins 1 and 8. **With the TC911, external offset voltage error canceling capacitors are not required.** On the TCS911 pins 1, 8 and 5 are not connected internally. The ICL7650 uses pin 5 as an optional output clamp connection. External chopper capacitors and clamp connections are not necessary with the TC911. External circuits connected to pins 1, 8 and 5 will have no effect. The TC911 can be quickly evaluated in existing ICL7650 designs. Since external capacitors are not required, system part count, assembly time, and total system cost are reduced. Reliability is increased and PC board layout eased by having the error storage capacitors integrated on the TC911 chip.

The TC911 pinout matches many existing op-amps: 741, LM101, LM108, OP05–OP08, OP20, OP21, ICL7650 and ICL7652. In many applications operating from +5V supplies the TC911 offers superior electrical performance and can be a functional pin-compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper-stabilization capacitors can be removed when retrofitting existing equipment designs.

Thermocouple Errors

Heating one joint of a loop made from two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop, an open circuit voltage (Seebeck voltage) can be measured. Junction temperature and metal type determine the magnitude. Typical values are 0.1 μV/°C to 10 μV/°C. Thermal-induced voltages can be many times larger than the TC911 offset voltage drift. Unless unwanted thermocouple potentials can be controlled, system performance will be less than optimum.

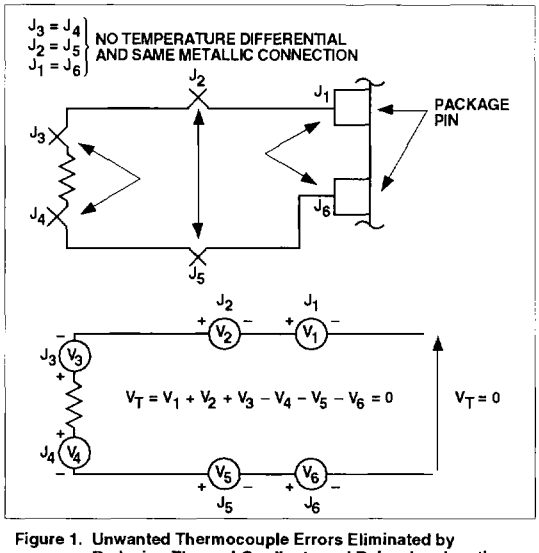


Figure 1. Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors are used. Low thermo-electric coefficient solder can reduce errors. A 60% Sn/36% Pb solder has 1/10 the thermal voltage of common 64% Sn/36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature, their summation will add to zero-canceling errors (Figure 1).

Shielding precision analog circuits from air currents — especially those caused by power dissipating components and fans — will minimize temperature gradients and thermocouple-induced errors.

Avoiding Latch-Up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and excessive power dissipation. TC911 power supplies should be established at the same time or before input signals are applied. If this is not possible input current should be limited to 0.1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers to establish "static safe" CMOS component handling areas. A partial company list is:

- 3M
  Static Control Systems Div
  223-23W EM Center
  St Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

Overload Recovery

The TC911 recovers quickly from the output saturation. Typical recovery time from positive output saturation is 20 ms. Negative output saturation recovery time is typically 5 ms.

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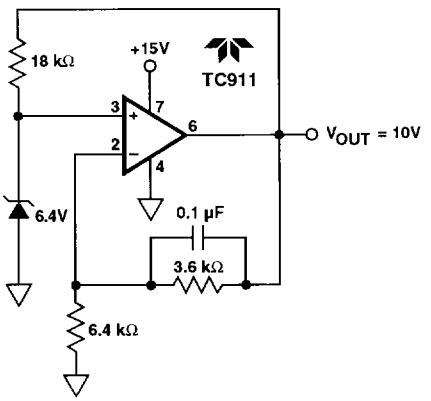
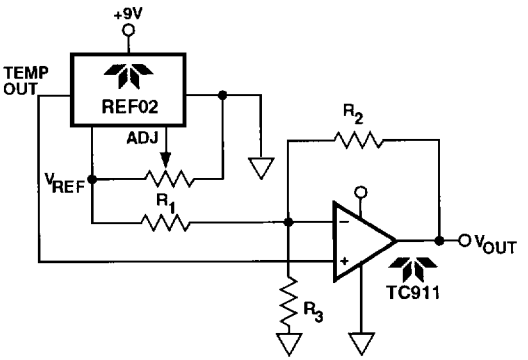
TC911

TYPICAL APPLICATIONS

10-Volt Precision Reference



Thermometer Circuit



$$V_{OUT} = V_{TEMP}\left[1 + R_2\left(\frac{R_3 + R_1}{R_3 \parallel R_1}\right)\right] - \left[V_{REF}\frac{R_2}{R_1}\right]$$

$$\frac{d\,V_{OUT}}{dT} = \left[1 + R_2\left(\frac{R_3 + R_1}{R_3 \parallel R_1}\right)\right]\frac{d\,(V_{TEMP})}{dT} \approx K\ (2.1\ mV/°C)$$

$$K = 1 + \frac{R_2}{R_3 \parallel R_1}$$

Programmable Gain Amplifier With Input Multiplexer