Integrated Circuit Systems, Inc.

ICS2510

Advance Information

3.3V Phase-Lock Loop Clock Driver

General Description

The ICS2510 is a high performance, low skew, low jitter clock driver. It uses a phase lock loop (PLL) technology to align, in both phase and frequency, the CLKIN signal with the CLKOUT signal. It is specifically designed for use with synchronous SDRAMs. The **ICS2510** operates at 3.3V VCC and drive up to ten clock loads.

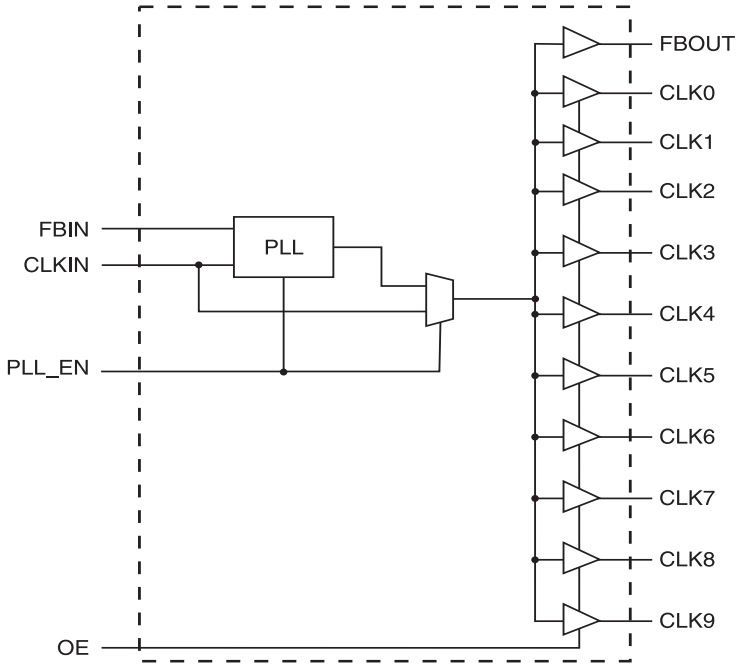
One bank of ten outputs provide low-skew, low-jitter copies of CLKIN. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLKIN. Outputs can be enabled or disabled via control (OE) inputs. When the OE inputs are high, the outputs align in phase and frequency with CLKIN; when the OE inputs are low, the outputs are disabled to the logic low state.

The **ICS2510** does not require external RC filter components. The loop filter for the PLL is include on-chip, minimizing component count, board space, and cost. The test mode shuts off the PLL and connects the input directly to the output buffer. This test mode, the **ICS2510** can be use as low skew fanout clock buffer device. The **ICS2510** comes in 24 pin 173mil Thin Shrink Small-Outline package (TSSOP) package.

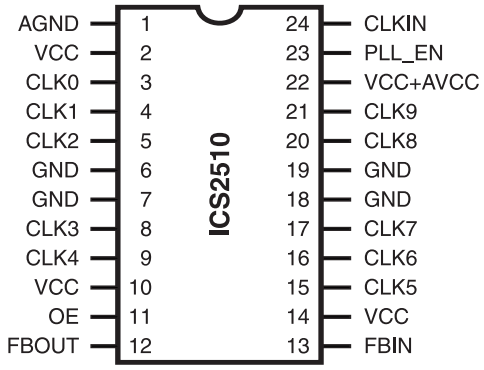
Features

- Meet PC SDRAM Registered DIMM Specification
- Spread Spectrum Clock Compatible
- Distributes one clock input to one bank of five and one bank of four outputs
- Operating frequency 25MHz to 125Mhz
- External feedback input (FBIN) terminal is used to synchrionize the outputs to the clock input
- No external RC network required
- Operates at 3.3V Vcc
- Plastic 24-pin 173mil TSSOP package

Block Diagram



Pin Configuration



24 Pin TSSOP

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	AGND	PWR	Analog Ground
2, 10, 14	VCC	PWR	Power Supply (3.3V)
3	CLK0[1]	OUT	Buffered clock output.
4	CLK1[1]	OUT	Buffered clock output.
5	CLK2[1]	OUT	Buffered clock output.
6, 7, 18, 19	GND	PWR	Ground
8	CLK3[1]	OUT	Buffered clock output.
9	CLK4[1]	OUT	Buffered clock output.
11	OE[2]	IN	Output enable (has internal pull_up). When high, normal operation. When low, clock outputs are disabled to a logic low state.
12	FBOUT[1]	OUT	Feedback output
13	FBIN	IN	Feedback input
15	CLK5[1]	OUT	Buffered clock output.
16	CLK6[1]	OUT	Buffered clock output.
17	CLK7[1]	OUT	Buffered clock output.
20	CLK8[1]	OUT	Buffered clock output.
21	CLK9[1]	OUT	Buffered clock output.
22	VCC+AVCC	PWR	Power Supply (3.3V) analog and digital supply.
23	PLL_EN	IN	PLL enable, when High, PLL is in normal operation. Whan Low PLL is bypassed and clock input CLKIN is buffered directly to the device outputs.
24	CLKIN	IN	Clock input

Notes:
1. Weak pull-down on all outputs
2. Weak pull-ups on these inputs

Functionality

INPUTS		OUTPUTS			PLL Shutdown
OE	PLL_EN	CLK (0:9)	FBOUT	Source	
0	1	0	Driven	PLL	N
1	1	Driven	Driven	PLL	N
Test Mode					
0	0	0	Driven	CLKIN	Y
1	0	Driven	Driven	CLKIN	Y

Test mode:
When PLL_EN is LOW
Shuts off the PLL and connects the input directly to the output buffers

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.6V, T_A = 0 – 70° C unless otherwise stated

Recommended operating condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Power Supply Voltage	3	3.3	3.6	V
VIH	High-level Input Voltage	2			V
VIL	Low-level Input Voltage			0.8	V
VI	Input Voltage	0		VCC	V
TA	Operating free-air temperature	0		70	℃

Electrical Characteristics Over Operating free-air Temperature Range

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VIK	Input clamp voltage	Vcc=3V,Ii=-18mA			-1.2	V
VOH	Output High Voltage	Vcc=MIN to MAX,Ii=-100uA	VCC-0.2			V
		Vcc=3V,Ii=-6mA	2.4			V
		Vcc=3V,Ii=-12mA	2.1			V
VOL	Output Low Voltage	Vcc=MIN to MAX,Ii=100uA			0.2	V
		Vcc=3V,Ii=6mA			0.55	V
		Vcc=3V,Ii=12mA			0.8	V
Ii	Input current	Vcc=3.6V,Vi=VCC or GND			±5	uA
Ipll_en	PLL_EN Supply Current	Vcc=3.6V,Vi=VCC or GND Io=0, Outputs:"L "or"H"			10	uA
ICC	Quiescent Supply Current (test mode)	Vcc=MAX,PLL_EN=LOW,CLKIN=LOW Oex=HIGH,all outputs unloaded				mA
ICC	Power Supply Current	VCC = 3.3 to 3.6V @ 100MHz all outputs unloaded			TBD	mA
Cin	Input Capacitance	Vcc=3.3V,Vi=VCC or GND		4		pF
Co	Output Capacitance	Vcc=3.3V,Vi=VCC or GND		6		pF

Note: For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating condidion

Timing requirements over recommended ranges of supply voltage and operating free-air temperature

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Fclk	Input clock frequency		25		125	MHz
	Input clock frequency duty cycle		40		60	%
	Stabilization time	After power up			1	ms

Note: Time required for the PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at Until phase lock is obtained, the specifications for parameters given in the switching characteristics table are not

Switching characteristics over recommended ranges of supply voltage and operating free-air temperature CL=30pF,RL=500ohms[1]

				VCC=3.3V ±0.165V			VCC=3.3V ±0.3V			
Symbol	Parameter	From(INPUT)	TO(OUTPUT)	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Tpe	Phase error	60MHz<CLKIN↑<125MHz	FBIN↑				-200		200	ps
Tpe[3]	Phase error-jitter	CLKIN↑=100MHz	FBIN↑	-150		150		0		ps
Tsk(0)[2]	Output-Output Skew	Any CLKOUT or FBOUT	Any CLKOUT or FBOUT				-200		200	ps
	Jitter(pk-pk)	CLKIN=66MHz to 100MHz	Any CLKOUT or FBOUT				-80		80	ps
	Jitter(cycle-cycle)	CLKIN=66MHz to 100MHz	Any CLKOUT or FBOUT				TBD		TBD	ps
Tdty	Duty cycle	CLKIN>60MHz	Any CLKOUT or FBOUT				45		55	%
Tr	Output rise time (0.4V to 2V)		Any CLKOUT or FBOUT		1.3	1.9	0.3		2.1	ns
Tf	Output fall time (2V to 0.4V)		Any CLKOUT or FBOUT		1.7	2.5	0.3		2.7	ns
Tpd	Propagation Delay PLL_EN=0,Vt=1.5v	CLKIN=66MHz to 100MHz	Any CLKOUT or FBOUT	1			1		TBD	ns

Notes:

1. Guaranteed by design and characterization. Not subject to 100% test.
2. The Tsk specification is only valid for equal loading of all outputs.
3. Phase error does not include jitter. The total phase error is -230 ps to 230 ps for the 5% VCC range.

PARAMETER MEASUREMENT INFORMATION

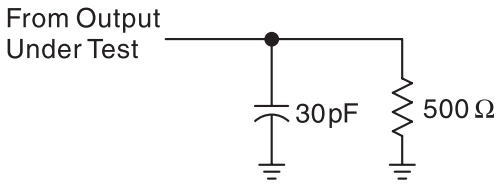


Figure 1. Load Circuit for Outputs

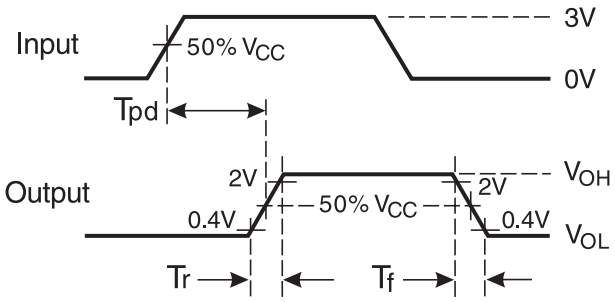


Figure 2. Voltage Waveforms Propagation Delay Times

Notes:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤100MHz, $Z_O = 50\Omega$, $T_r \leq 1.2ns$, $T_f \leq 1.2ns$.
3. The outputs are measured one at a time with one transition per measurement.

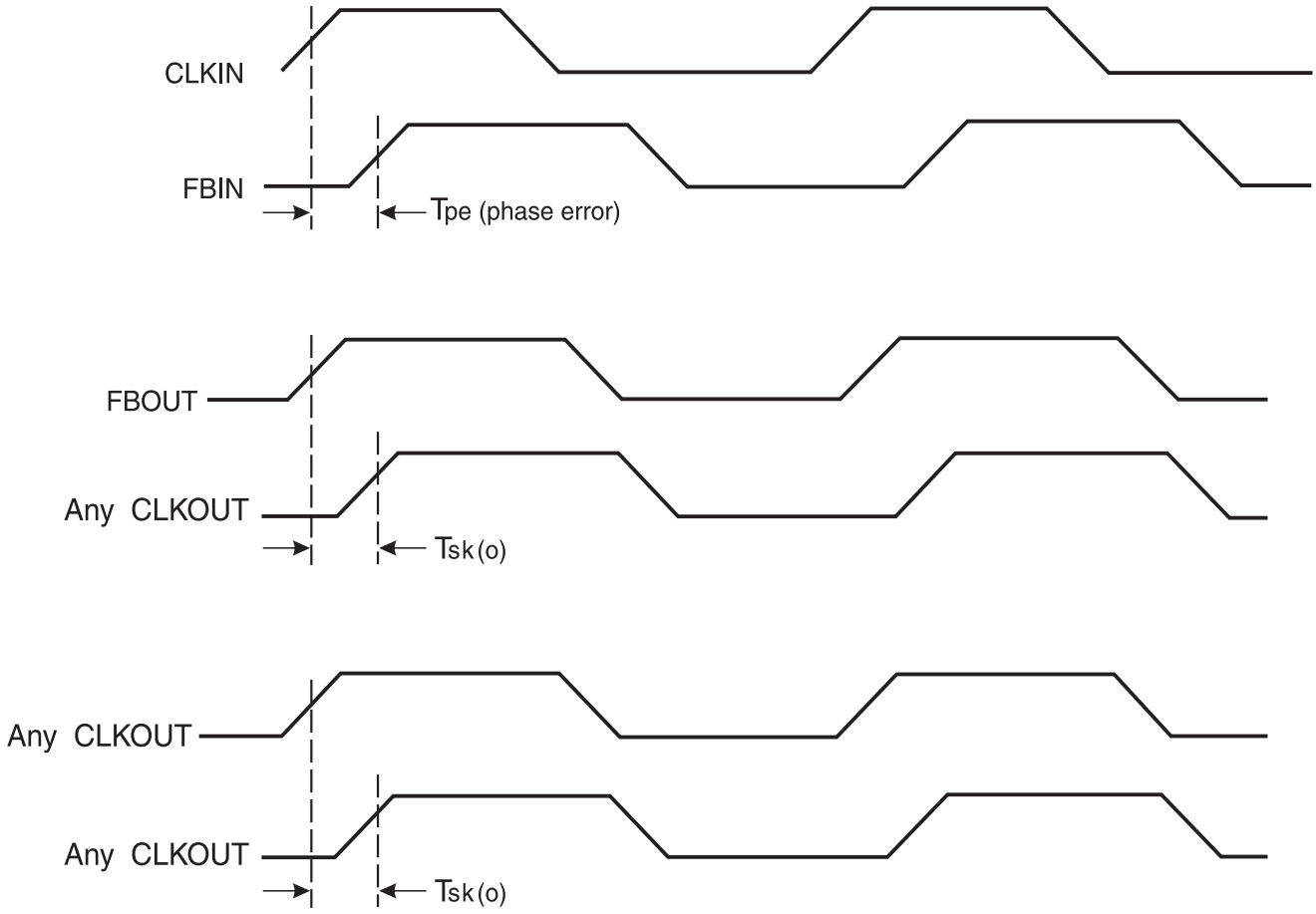
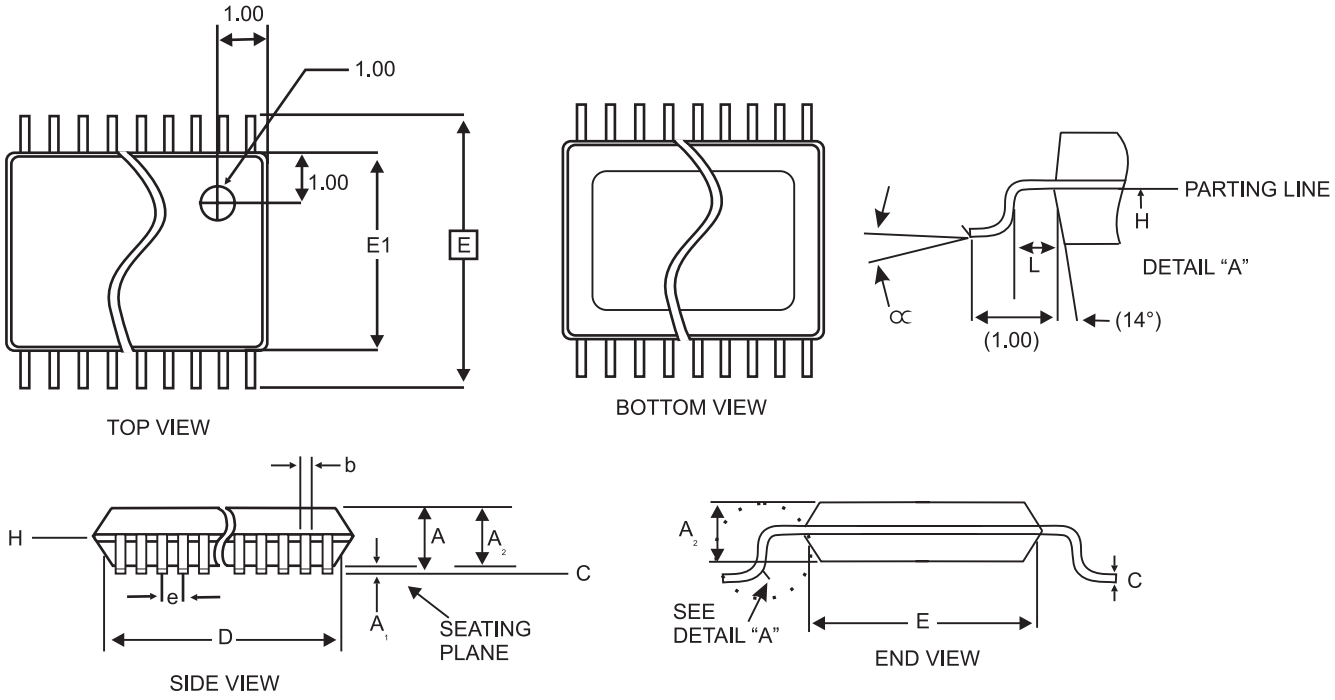


Figure 3. Phase Error and Skew Calculations



173 mil TSSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D	N
	MIN.	NOM.	MAX.			
A	—	—	1.10	AA/AAT	3.00 BSC	8
A1	0.05	—	0.15	AB-1/ABT	5.00 BSC	14
A2	0.85	0.90	0.95	AB/ABT	5.00 BSC	16
b	0.19	—	0.30	AC/ACT	6.50 BSC	20
C	0.09	—	0.20	AD/ADT	7.80 BSC	24
D	See Variations			AE/AET	9.70 BSC	28
E1	4.30	4.40	4.50			
e	0.65 BSC					
E	6.40 BSC					
L	0.50	0.60	0.70			
N	See Variations					
P	See Variations					
P1	See Variations					
α	0°	—	8°			

Diminisions are in millimeters
173TSSOP_AN

Ordering Information

ICS2510G

Example:

ICS XXXX Y F

Package Type
G=TSSOP

Revision Designator

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS= Standard Device