

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54ALS640A THRU SN54ALS645A, SN54AS640 THRU SN54AS645 SN74ALS640A THRU SN74ALS645A, SN74AS640 THRU SN74AS645 OCTAL BUS TRANSCEIVERS

D2661, DECEMBER 1983—REVISED MAY 1986

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'ALS640A, 'AS640	3-State	Inverting
'ALS641A, 'AS641	Open-Collector	True
'ALS642A, 'AS642	Open-Collector	Inverting
'ALS643A, 'AS643	3-State	True and Inverting
'ALS644A, 'AS644	Open-Collector	True and Inverting
'ALS645A, 'AS645	3-State	True

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so the buses are effectively isolated.

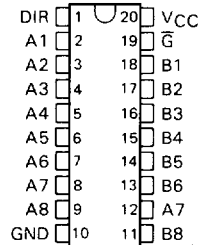
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

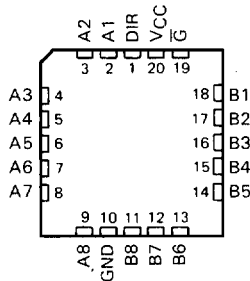
FUNCTION TABLE

CONTROL INPUTS		OPERATION		
\bar{G}	DIR	'ALS640A, 'AS640	'ALS641A, 'AS641	'ALS643A, 'AS643
L	L	\bar{B} data to A bus	B data to A bus	B data to A bus
L	H	\bar{A} data to B bus	A data to B bus	\bar{A} data to B bus
H	X	Isolation	Isolation	Isolation

SN54ALS', SN54AS' ... J PACKAGE
SN74ALS', SN74AS' ... DW OR N PACKAGE
(TOP VIEW)

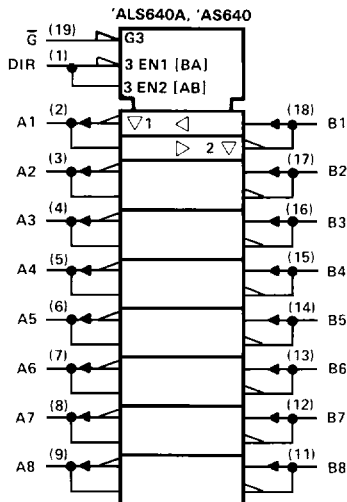


SN54ALS', SN54AS' ... FK PACKAGE
(TOP VIEW)

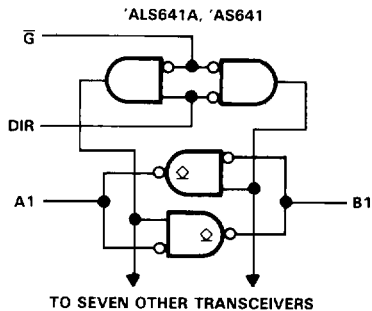
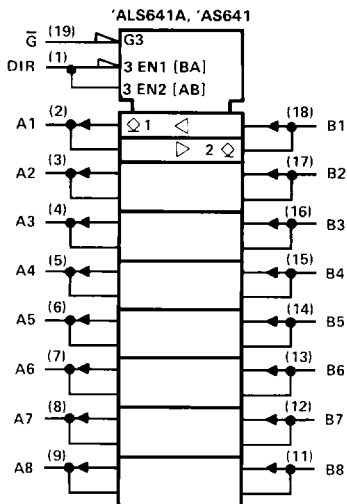
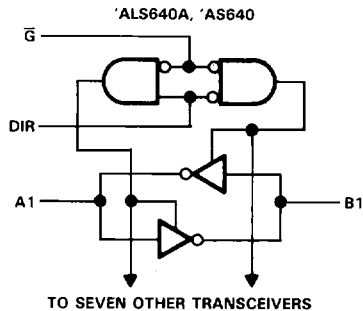


**SN54ALS640A, SN54ALS641A, SN54AS640, SN54AS641
SN74ALS640A, SN74ALS641A, SN74AS640, SN74AS641
OCTAL BUS TRANSCEIVERS**

logic symbols†



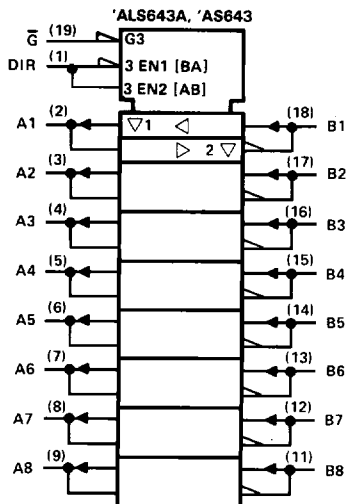
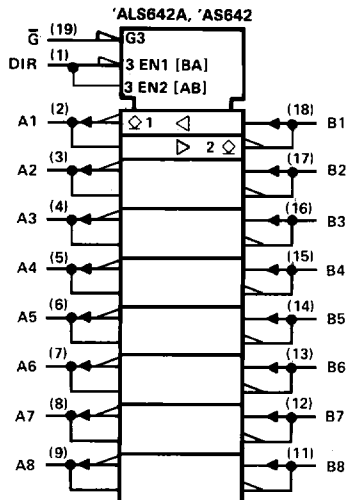
logic diagrams (positive logic)



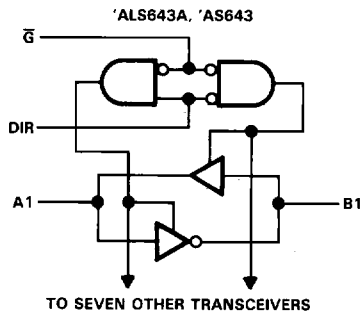
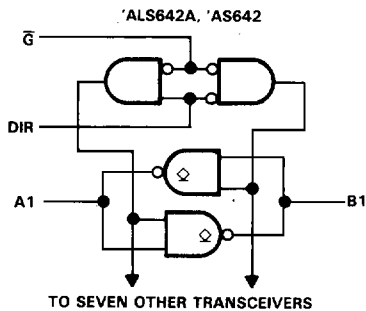
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

**SN54ALS642A, SN54ALS643A, SN54AS642, SN54AS643
SN74ALS642A, SN74ALS643A, SN74AS642, SN74AS643
OCTAL BUS TRANSCEIVERS**

logic symbols†



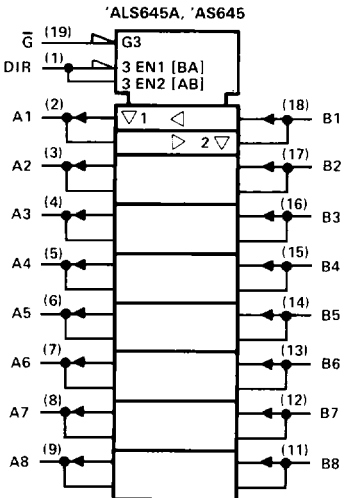
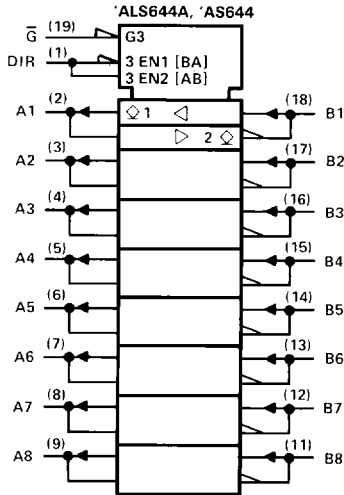
logic diagrams (positive logic)



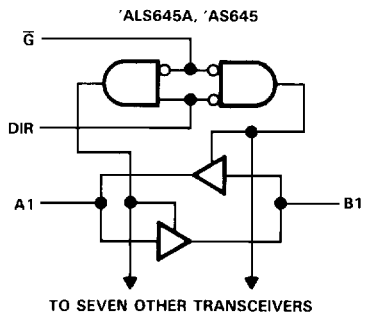
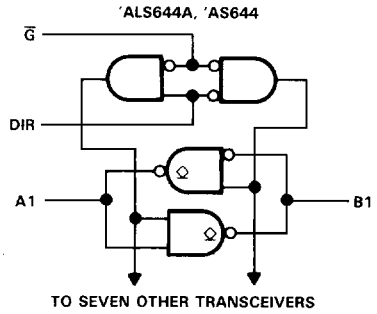
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

**SN54ALS644A, SN54ALS645A, SN54AS644, SN54AS645
 SN74ALS644A, SN74ALS645A, SN74AS644, SN74AS645
 OCTAL BUS TRANSCEIVERS**

logic symbols†



logic diagrams (positive logic)



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ALS and AS Circuits

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

SN54ALS640A, SN54ALS643A, SN54ALS645A SN74ALS640A, SN74ALS643A, SN74ALS645A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS640A, SN54ALS643A, SN54ALS645A	-55 °C to 125 °C
SN74ALS640A, SN74ALS643A, SN74ALS645A	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54ALS640A SN54ALS643A SN54ALS645A			SN74ALS640A SN74ALS643A SN74ALS645A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.7			0.8			V
I_{OH}	High-level output current	-12			-15			mA
I_{OL}	Low-level output current	12			24			mA
					48†			
T_A	Operating free-air temperature	-55			125			°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS640A-1, SN74ALS643A-1, and SN74ALS645A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS ¹			SN74ALS ¹			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA	-1.5			-1.5			V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5$ V, $I_{OH} = -3$ mA	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5$ V, $I_{OH} = -12$ mA	2						
	$V_{CC} = 4.5$ V, $I_{OH} = -15$ mA				2			
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA	0.25			0.4	0.25	0.4	V
	$V_{CC} = 4.5$ V, $I_{OL} = 24$ mA ($I_{OL} = 48$ mA for -1 versions)				0.35	0.5		
I_I	Control inputs	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			mA
	A or B ports	$V_{CC} = 5.5$ V, $V_I = 5.5$ V			0.1			
I_{IH}	Control inputs	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			μ A
	A or B ports‡				20			
I_{IL}	Control inputs	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.1			mA
	A or B ports‡				-0.1			
I_{O1}	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	-30		-112	-30		-112	mA
I_{CC}	'ALS640A	$V_{CC} = 5.5$ V	Outputs high	19	35	19	30	mA
			Outputs low	27	45	27	40	
			Outputs disabled	28	48	28	43	
			Outputs high	25	37	25	35	
	'ALS643A		Outputs low	33	47	33	45	
			Outputs disabled	35	50	35	48	
	'ALS645A		Outputs high	30	48	30	45	
			Outputs low	36	60	36	55	
	Outputs disabled	38	63	38	58			

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

† The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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ALS and AS Circuits

**SN54ALS640A, SN54ALS643A, SN54ALS645A
SN74ALS640A, SN74ALS643A, SN74ALS645A
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

'ALS640A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS640A		SN74ALS640A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	14	2	11	ns
t_{PHL}			2	13	2	10	
t_{PZH}	\bar{G}	A or B	5	25	5	21	ns
t_{PZL}			8	27	8	24	
t_{PHZ}	\bar{G}	A or B	2	12	2	10	ns
t_{PLZ}			3	20	3	15	

'ALS643A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS643A		SN74ALS643A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	13	ns
t_{PHL}			2	13	2	11	
t_{PLH}	B	A	2	15	2	13	ns
t_{PHL}			2	13	2	11	
t_{PZH}	\bar{G}	A	5	28	5	25	ns
t_{PZL}			5	28	5	25	
t_{PHZ}	\bar{G}	A	2	12	2	10	ns
t_{PLZ}			3	22	3	17	
t_{PZH}	\bar{G}	B	5	28	5	25	ns
t_{PZL}			5	28	5	25	
t_{PHZ}	\bar{G}	B	2	12	2	10	ns
t_{PLZ}			3	22	3	17	

'ALS645A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS645A		SN74ALS645A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	19	3	10	ns
t_{PHL}			1	14	3	10	
t_{PZH}	\bar{G}	A or B	2	30	5	20	ns
t_{PZL}			2	29	5	20	
t_{PHZ}	\bar{G}	A or B	2	14	2	10	ns
t_{PLZ}			2	30	4	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 ALS and AS Circuits

SN54ALS641A, SN54ALS642A, SN54ALS644A SN74ALS641A, SN74ALS642A, SN74ALS644A OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs and I/O ports	7 V
Operating free-air temperature range:	
SN54ALS641A, SN54ALS642A, SN54ALS644A	-55 °C to 125 °C
SN74ALS641A, SN74ALS642A, SN74ALS644A	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54ALS641A SN54ALS642A SN54ALS644A			SN74ALS641A SN74ALS642A SN74ALS644A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output current			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	-55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS641A-1, SN74ALS642A-1, and SN74ALS644A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS641A SN54ALS642A SN54ALS644A			SN74ALS641A SN74ALS642A SN74ALS644A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA		-1.5			-1.5		V
I_{OH}	$V_{CC} = 4.5$ V, $V_{OH} = 5.5$ V			0.1			0.1	mA
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA		0.25	0.4		0.25	0.4	V
	$V_{CC} = 4.5$ V, $I_{OL} = 24$ mA ($I_{OL} = 48$ mA for -1 versions)					0.35	0.5	
I_I	Control inputs $V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			0.1	mA
	A or B ports $V_{CC} = 5.5$ V, $V_I = 5.5$ V			0.1			0.1	
I_{IH}	Control inputs $V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			20	µA
	A or B ports§ $V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			20	
I_{IL}	Control inputs $V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.1			-0.1	mA
	A or B ports§ $V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.1			-0.1	
I_{CC}	'ALS641A 'ALS642A 'ALS644A	$V_{CC} = 5.5$ V	Outputs high	25	40	25	37	mA
			Outputs low	33	50	33	47	
			Outputs high	8	15	8	15	
			Outputs low	18	28	18	28	
			Outputs high	16	32	16	29	
			Outputs low	25	44	25	40	

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

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ALS and AS Circuits

**SN54ALS641A, SN54ALS642A, SN54ALS644A
SN74ALS641A, SN74ALS642A, SN74ALS644A
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS**

'ALS641A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V,}$ $C_L = 50\text{ pF,}$ $R_L = 680\ \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS641A		SN74ALS641A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	30	5	25	ns
t_{PHL}			3	23	3	18	
t_{PLH}	\bar{G}	A or B	8	35	8	30	ns
t_{PHL}			8	35	8	30	
t_{PLH}	DIR	A or B	8	37	8	32	ns
t_{PHL}			8	37	8	32	

'ALS642A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V,}$ $C_L = 50\text{ pF,}$ $R_L = 680\ \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS642A		SN74ALS642A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	10	35	10	30	ns
t_{PHL}			5	25	5	22	
t_{PLH}	\bar{G} or DIR	A or B	10	35	10	30	ns
t_{PHL}			15	43	15	38	

'ALS644A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V,}$ $C_L = 50\text{ pF,}$ $R_L = 680\ \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS644A		SN74ALS644A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	10	35	10	30	ns
t_{PHL}			5	25	5	22	
t_{PLH}	B	A	10	35	10	30	ns
t_{PHL}			5	23	5	21	
t_{PLH}	\bar{G}	A	8	35	8	30	ns
t_{PHL}			10	38	10	35	
t_{PLH}	\bar{G}	B	8	31	8	26	ns
t_{PHL}			15	40	15	35	
t_{PLH}	DIR	A	8	31	8	26	ns
t_{PHL}			10	40	10	35	
t_{PLH}	DIR	B	10	35	10	30	ns
t_{PHL}			15	40	15	35	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 ALS and AS Circuits

SN54AS640, SN54AS643, SN54AS645 SN74AS640, SN74AS643, SN74AS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range:	
SN54AS640, SN54AS643, SN54AS645	-55 °C to 125 °C
SN74AS640, SN74AS643, SN74AS645	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54AS640 SN54AS643 SN54AS645			SN74AS640 SN74AS643 SN74AS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.8			V
I_{OH}	High-level output current				-12			mA
I_{OL}	Low-level output current				64			mA
T_A	Operating free-air temperature	-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS ¹			SN74AS ¹			UNIT
		MIN	TYP ²	MAX	MIN	TYP ²	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$	-1.2			-1.2			V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2.4						
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -15 \text{ mA}$				2.4			
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 48 \text{ mA}$	0.30			0.55			V
	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 64 \text{ mA}$				0.35			
I_I	Control inputs $V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$				0.1			mA
	A or B ports $V_{CC} = 5.5 \text{ V}$, $V_I = 5.5 \text{ V}$				0.1			
I_{IH}	Control inputs $V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$				20			μA
	A or B ports [‡]				70			
I_{IL}	Control inputs $V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$				-0.5			mA
	A or B ports [‡]				-0.75			
I_O^{\S}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-50		-150	-50		-150	mA
I_{CC}	'AS640	$V_{CC} = 5.5 \text{ V}$	Outputs high	37	58	37	58	mA
			Outputs low	78	123	78	123	
			Outputs disabled	51	80	51	80	
	'AS643		Outputs high	48	79	48	79	
			Outputs low	88	143	88	143	
			Outputs disabled	61	100	61	100	
	'AS645		Outputs high	62	97	62	97	
			Outputs low	95	149	95	149	
			Outputs disabled	79	123	79	123	

¹All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

²For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

³The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54AS640, SN54AS643, SN54AS645
SN74AS640, SN74AS643, SN74AS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

'AS640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS640		SN74AS640		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	8	2	7	ns
t_{PHL}			2	7	2	6	
t_{PZH}	\bar{G}	A or B	2	10	2	8	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	\bar{G}	A or B	2	9	2	8	ns
t_{PLZ}			2	16	2	13	

'AS643 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS643		SN74AS643		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	10	2	8	ns
t_{PHL}			2	7.5	2	7	
t_{PLH}	B	A	2	11.5	2	10	ns
t_{PHL}			2	10	2	9	
t_{PZH}	\bar{G}	A	2	13	2	11	ns
t_{PZL}			2	13	2	11	
t_{PHZ}	\bar{G}	A	2	8.5	2	7.5	ns
t_{PLZ}			2	12	2	10.5	
t_{PZH}	\bar{G}	B	2	11.5	2	10	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	\bar{G}	B	2	8	2	7	ns
t_{PLZ}			2	12	2	10	

'AS645 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS645		SN74AS645		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	11	2	9.5	ns
t_{PHL}			2	10.5	2	9	
t_{PZH}	\bar{G}	A or B	2	12	2	11	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	\bar{G}	A or B	2	8	2	7	ns
t_{PLZ}			2	13	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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SN54AS641, SN54AS642, SN54AS644
SN74AS641, SN74AS642, SN74AS644
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs and I/O ports	7 V
Operating free-air temperature range:	
SN54AS641, SN54AS642, SN54AS644	-55°C to 125°C
SN74AS641, SN74AS642, SN74AS644	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS641 SN54AS642 SN54AS644			SN74AS641 SN74AS642 SN74AS644			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output current			5.5			5.5	V
I_{OL}	Low-level output current			48			64	V
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS641 SN54AS642 SN54AS644			SN74AS641 SN74AS642 SN74AS644			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
I_{OH}	$V_{CC} = 4.5\text{ V}$, $V_{OH} = 5.5\text{ V}$			0.1			0.1	mA
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$		0.3	0.55				V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 64\text{ mA}$				0.35	0.55		
I_I	Control inputs $V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			0.1	mA
	A or B ports $V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$			0.1			0.1	
I_{IH}	Control inputs $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			20	μA
	A or B ports [‡] $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			70			70	
I_{IL}	Control inputs $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.5			-0.5	mA
	A or B ports [‡] $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.75			-0.75	
I_{CC}	'AS641	Outputs high		50	82	50	82	mA
		Outputs low		84	136	84	136	
	'AS642	Outputs high		25	42	25	42	
		Outputs low		64	104	64	104	
	'AS644	Outputs high		38	62	38	62	
		Outputs low		76	124	76	124	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

SN54AS641, SN54AS642, SN54AS644
SN74AS641, SN74AS642, SN74AS644
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

'AS641 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS641		SN74AS641		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	23	5	21	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	\bar{G}	A or B	5	24	5	21	ns
t_{PHL}			1	10	1	9	
t_{PLH}	DIR	A or B	5	26	5	22	ns
t_{PHL}			1	11	1	10	

'AS642 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS642		SN74AS642		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	5	28.5	5	24	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	\bar{G}	A or B	5	25	5	22	ns
t_{PHL}			1	11	1	10	
t_{PLH}	DIR	A or B	5	26.5	5	23.5	ns
t_{PHL}			1	12.5	1	11.5	

'AS644 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS644		SN74AS644		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5	28.5	5	24	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	5	23	5	21	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	\bar{G}	A or B	5	24	5	21	ns
t_{PHL}			1	10	1	9	
t_{PLH}	DIR	A or B	5	26	5	22	ns
t_{PHL}			1	11	1	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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