8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT853

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector $\overline{\text{ERROR}}$ output
- Functionally equivalent to AMD AM29853
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT853 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT853 is an octal transceiver with a parity generator/checker and is intended for bus-oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	6.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

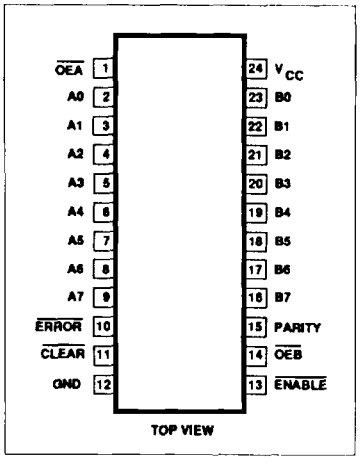
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT853N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT853D

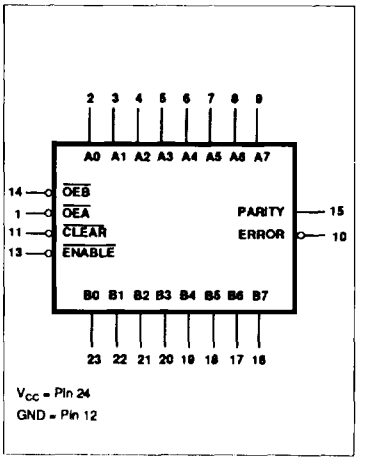
The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a latch. The error data can then be passed, stored, cleared, or sampled depending on the $\overline{\text{ENABLE}}$ and $\overline{\text{CLEAR}}$ control signals.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

PIN CONFIGURATION



LOGIC SYMBOL



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PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 - A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3-State inputs/outputs
B0 - B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3-State inputs/outputs
$\overline{OEA}$	1	Enables the A outputs when Low
$\overline{OEB}$	14	Enables the B outputs when Low
PARITY	15	Parity output
$\overline{ERROR}$	10	Error output
$\overline{CLEAR}$	11	Clears the error flag register when Low
$\overline{ENABLE}$	13	Enable input (active low)
GND	12	Ground (0V)
V_{CC}	24	Positive supply voltage

FUNCTION TABLE

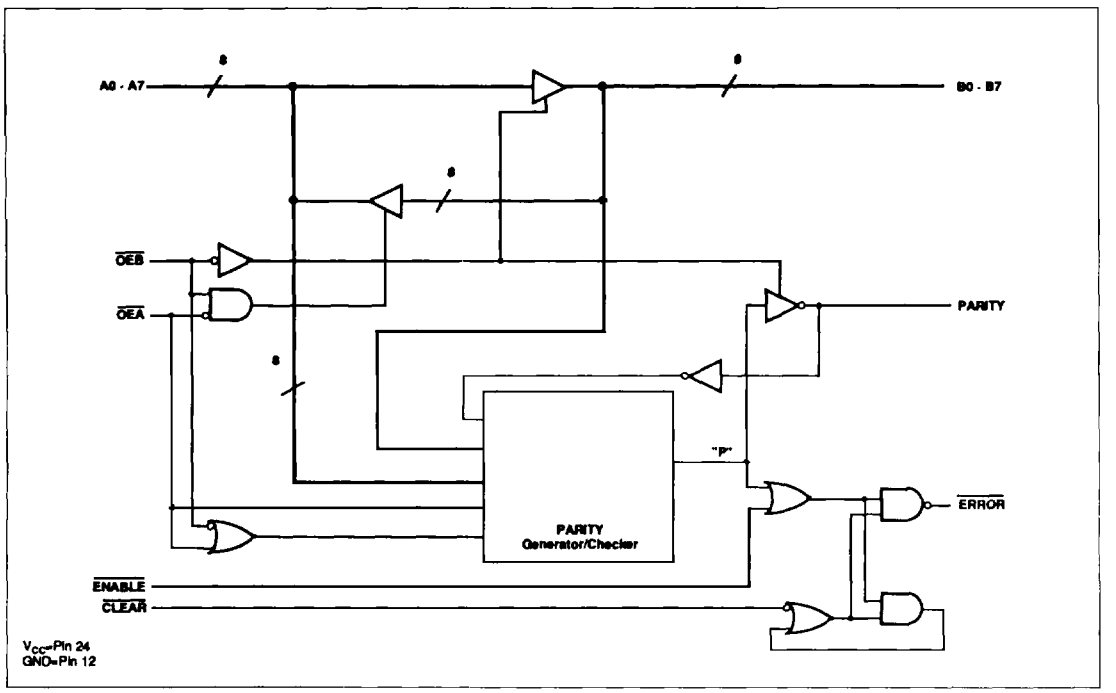
MODE	INPUTS						OUTPUT AND I/O			
	$\overline{OEB}$	$\overline{OEA}$	$\overline{CLEAR}$	CP	An Σ of Highs	Bn† Σ of Highs	A	B	PARITY	$\overline{ERROR}$‡
A data to B bus and generate parity	L	H	X	X	Odd Even	NA	NA	A	L H	NA
B data to A bus and check parity	H	L	H	↑	NA	Odd Even	B	NA	NA	H L
Clear error flag register	X	X	L	X	X	X	X	NA	NA	H
A bus and B bus disabled §	H	H	H L H H	 ‡ ‡	X X Odd Even	X	Z	Z	Z	NC H H L
A data to B bus and generate inverted parity (Forced-error)	L	L	X	X	Odd Even	NA	NA	A	H L	NA

ERROR FLAG FUNCTION TABLE

MODE	INPUTS		Internal node Point "P"	OUTPUT
	$\overline{CLEAR}$	$\overline{ENABLE}$		$\overline{ERROR}$
Transparent	L L	L L	L H	L H
Sample	H H	L L	L H	L H
Clear	L	H	X	H
Store	H H	H H	L H	L H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
NA = Not applicable
NC = No change
Z = High-impedance "OFF" state
† = Summation of High-level inputs includes PARITY along with Bn inputs
‡ = Output states shown assume the $\overline{ERROR}$ output was previously High
§ In this mode, the ERROR output, when clocked, shows inverted parity of the A bus
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
I_{OH}	High-level output current $\overline{ERROR}$ only		V_{CC} = 4.5V; V_{OH} = 4.5V; V_I = V_{IL} or V_{IH}			20		20	µA
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		
			V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]		V_{CC} = 5.5V; V_O = 2.5V	-50	-80	-180	-50	-180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.