

## 74LVTH16500

### Low Voltage 18-Bit Universal Bus Transceivers with Bushold and 3-STATE Outputs

#### General Description

The LVTH16500 is an 18-bit universal bus transceiver combining D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs.

The LVTH16500 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

The transceiver is designed for low voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH16500 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

#### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power up/down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 16500
- ESD Performance:
  - Human-Body Model > 2000V
  - Machine Model > 200V
  - Charged-Device Model > 1000V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

#### Ordering Code:

Order Number	Package Number	Package Description
74LVTH16500GX (Note 1)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LVTH16500MEA (Note 2)	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVTH16500MTD (Note 2)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

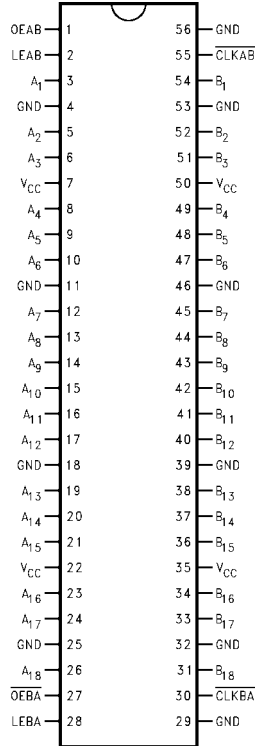
**Note 1:** BGA package available in Tape and Reel only.

**Note 2:** Devices also available in Tape and Reel. Specify by appending the suffix "X" to the ordering code.

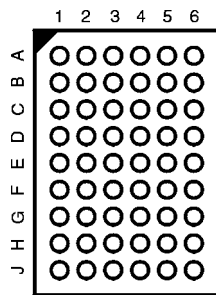
74LVTH16500 Low Voltage 18-Bit Universal Bus Transceivers with Bushold and 3-STATE Outputs

## Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

## Pin Descriptions

Pin Names	Description
A <sub>1</sub> -A <sub>18</sub>	Data Register A Inputs/3-STATE Outputs
B <sub>1</sub> -B <sub>18</sub>	Data Register B Inputs/3-STATE Outputs
CLKAB, CLKBA	Clock Pulse Inputs
LEAB, LEBA	Latch Enable Inputs
OEAB, OEBA	Output Enable Inputs

## FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	A <sub>2</sub>	A <sub>1</sub>	OEAB	GND	B <sub>1</sub>	B <sub>2</sub>
<b>B</b>	A <sub>4</sub>	A <sub>3</sub>	LEAB	CLKAB	B <sub>3</sub>	B <sub>4</sub>
<b>C</b>	A <sub>6</sub>	A <sub>5</sub>	V <sub>CC</sub>	V <sub>CC</sub>	B <sub>5</sub>	B <sub>6</sub>
<b>D</b>	A <sub>8</sub>	A <sub>7</sub>	GND	GND	B <sub>7</sub>	B <sub>8</sub>
<b>E</b>	A <sub>10</sub>	A <sub>9</sub>	GND	GND	B <sub>9</sub>	B <sub>10</sub>
<b>F</b>	A <sub>12</sub>	A <sub>11</sub>	GND	GND	B <sub>11</sub>	B <sub>12</sub>
<b>G</b>	A <sub>14</sub>	A <sub>13</sub>	V <sub>CC</sub>	V <sub>CC</sub>	B <sub>13</sub>	B <sub>14</sub>
<b>H</b>	A <sub>16</sub>	A <sub>15</sub>	OEAB	CLKBA	B <sub>15</sub>	B <sub>16</sub>
<b>J</b>	A <sub>17</sub>	A <sub>18</sub>	LEBA	GND	B <sub>18</sub>	B <sub>17</sub>

## Function Table (Note 3)

Inputs				Output
OEAB	LEAB	CLKAB	A <sub>n</sub>	B <sub>n</sub>
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B <sub>0</sub> (Note 4)
H	L	L	X	B <sub>0</sub> (Note 5)

H = HIGH Voltage Level      L = LOW Voltage Level  
 X = Immaterial                  Z = High Impedance  
 ↓ = HIGH-to-LOW Clock Transition

**Note 3:** A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA. OEBA is active LOW.

**Note 4:** Output level before the indicated steady-state input conditions were established.

**Note 5:** Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.

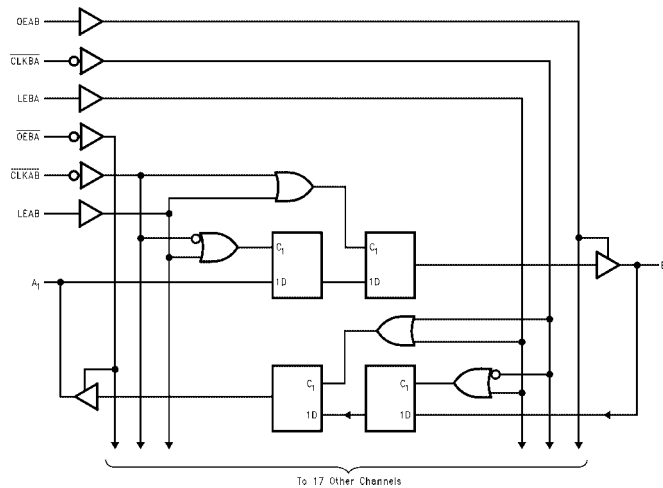
## Functional Description

For A-to-B data flow, the device operates in the transparent mode when  $\overline{LEAB}$  is HIGH. When  $\overline{LEAB}$  is LOW, the A data is latched if  $\overline{CLKAB}$  is held at a HIGH or LOW logic level. If  $\overline{LEAB}$  is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of  $\overline{CLKAB}$ . Output-enable OEAB is active-HIGH. When OEAB is

HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses  $\overline{OEBA}$ ,  $\overline{LEBA}$ , and  $\overline{CLKBA}$ . The output enables are complementary (OEAB is active-HIGH and  $\overline{OEBA}$  is active-LOW).

## Logic Diagram



Absolute Maximum Ratings (Note 6)				
Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +4.6		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 7)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
$I_O$	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 64$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 128$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}C$
Recommended Operating Conditions				
Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage	2.7	3.6	V
$V_I$	Input Voltage	0	5.5	V
$I_{OH}$	HIGH-Level Output Current		-32	mA
$I_{OL}$	LOW-Level Output Current		64	mA
$T_A$	Free-Air Operating Temperature	-40	85	$^{\circ}C$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V
<p><b>Note 6:</b> Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.</p> <p><b>Note 7:</b> <math>I_O</math> Absolute Maximum Rating must be observed.</p>				

DC Electrical Characteristics							
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Conditions	
			Min	Max			
V <sub>IK</sub>	Input Clamp Diode Voltage	2.7		-1.2	V	I <sub>I</sub> = -18 mA	
V <sub>IH</sub>	Input HIGH Voltage	2.7-3.6	2.0		V	V <sub>O</sub> ≤ 0.1V or	
V <sub>IL</sub>	Input LOW Voltage	2.7-3.6		0.8		V <sub>O</sub> ≥ V <sub>CC</sub> - 0.1V	
V <sub>OH</sub>	Output HIGH Voltage	2.7-3.6	V <sub>CC</sub> - 0.2		V	I <sub>OH</sub> = -100 μA	
		2.7	2.4		V	I <sub>OH</sub> = -8 mA	
		3.0	2.0		V	I <sub>OH</sub> = -32 mA	
V <sub>OL</sub>	Output LOW Voltage	2.7		0.2	V	I <sub>OL</sub> = 100 μA	
		2.7		0.5	V	I <sub>OL</sub> = 24 mA	
		3.0		0.4	V	I <sub>OL</sub> = 16 mA	
		3.0		0.5	V	I <sub>OL</sub> = 32 mA	
		3.0		0.55	V	I <sub>OL</sub> = 64 mA	
I <sub>I(HOLD)</sub>	Bushold Input Minimum Drive	3.0	75		μA	V <sub>I</sub> = 0.8V	
			-75		μA	V <sub>I</sub> = 2.0V	
I <sub>I(OD)</sub>	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 8)	
			-500		μA	(Note 9)	
I <sub>I</sub>	Input Current	3.6		10	μA	V <sub>I</sub> = 5.5V	
	Control Pins	3.6		±1	μA	V <sub>I</sub> = 0V or V <sub>CC</sub>	
	Data Pins	3.6		-5	μA	V <sub>I</sub> = 0V	
I <sub>OFF</sub>	Power Off Leakage Current	0		±100	μA	0V ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V	
I <sub>PU/PD</sub>	Power Up/Down 3-STATE Output Current	0-1.5V		±100	μA	V <sub>O</sub> = 0.5V to 3.0V V <sub>I</sub> = GND or V <sub>CC</sub>	
I <sub>OZL</sub>	3-STATE Output Leakage Current	3.6		-5	μA	V <sub>O</sub> = 0.0V	
I <sub>OZH</sub>	3-STATE Output Leakage Current	3.6		5	μA	V <sub>O</sub> = 3.6V	
I <sub>OZH+</sub>	3-STATE Output Leakage Current	3.6		10	μA	V <sub>CC</sub> < V <sub>O</sub> ≤ 5.5V	
I <sub>CCH</sub>	Power Supply Current	3.6		0.19	mA	Outputs HIGH	
I <sub>CCL</sub>	Power Supply Current	3.6		5	mA	Outputs LOW	
I <sub>CCZ</sub>	Power Supply Current	3.6		0.19	mA	Outputs Disabled	
I <sub>CCZ+</sub>	Power Supply Current	3.6		0.19	mA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled	
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 10)	3.6		0.2	mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND	
<p><b>Note 8:</b> An external driver must source at least the specified current to switch from LOW-to-HIGH.</p> <p><b>Note 9:</b> An external driver must sink at least the specified current to switch from HIGH-to-LOW.</p> <p><b>Note 10:</b> This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.</p>							
Dynamic Switching Characteristics (Note 11)							
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 12)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 12)
<p><b>Note 11:</b> Characterized in SSOP package. Guaranteed parameter, but not tested.</p> <p><b>Note 12:</b> Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.</p>							

## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, C_L = 50 \text{ pF}, R_L = 500 \Omega$				Units
		$V_{CC} = 3.3 \pm 0.3\text{V}$		$V_{CC} = 2.7\text{V}$		
		Min	Max	Min	Max	
$f_{MAX}$	CLKAB or CLKBA to B or A	150		150		MHz
$t_{PLH}$	Propagation Delay	1.3	5.2	1.3	5.8	ns
$t_{PHL}$	Data to Outputs	1.3	4.7	1.3	5.3	
$t_{PLH}$	Propagation Delay	1.5	5.5	1.5	6.3	ns
$t_{PHL}$	LEBA or LEAB to B or A	1.5	5.1	1.5	5.7	
$t_{PLH}$	Propagation Delay	1.3	5.8	1.3	6.9	ns
$t_{PHL}$	CLKBA or CLKAB to B or A	1.2	5.0	1.3	5.9	
$t_{PZH}$	Output Enable Time	1.2	5.0	1.3	5.7	ns
$t_{PZL}$		1.3	5.5	1.3	6.5	
$t_{PHZ}$	Output Disable Time	1.7	6.0	1.7	6.7	ns
$t_{PLZ}$		1.6	5.8	1.7	6.3	
$t_{SU}$	Setup Time	A before $\overline{\text{CLKAB}}$	2.9		2.9	ns
		B before $\overline{\text{CLKBA}}$	2.9		2.9	
		A or B before LE, $\overline{\text{CLK HIGH}}$	1.8		0.9	
		A or B before LE, $\overline{\text{CLK LOW}}$	2.9		2.3	
$t_H$	Hold Time	A or B after $\overline{\text{CLK}}$	0.5		0.9	ns
		A or B after LE	1.6		1.6	
$t_W$	Pulse Duration	LE HIGH	3.3		3.3	ns
		$\overline{\text{CLK HIGH}}$ or LOW	3.3		3.3	
$t_{OSLH}$	Output to Output Skew (Note 13)		1.0		1.0	ns
$t_{OSHL}$			1.0		1.0	

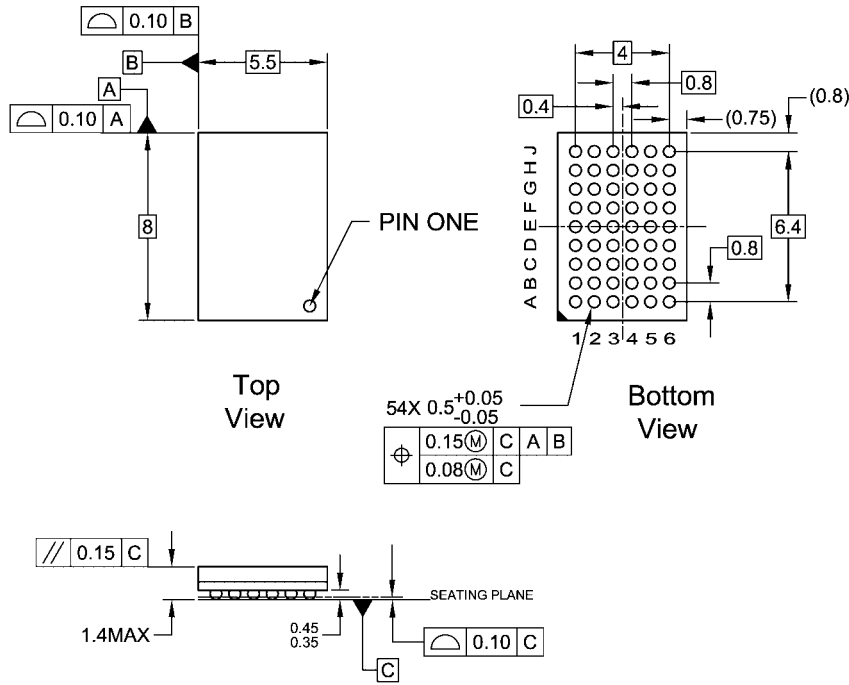
**Note 13:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ).

## Capacitance (Note 14)

Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = 0\text{V}, V_I = 0\text{V}$ or $V_{CC}$	4	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.0\text{V}, V_O = 0\text{V}$ or $V_{CC}$	8	pF

**Note 14:** Capacitance is measured at frequency  $f = 1 \text{ MHz}$ , per MIL-STD-883, Method 3012.

**Physical Dimensions** inches (millimeters) unless otherwise noted

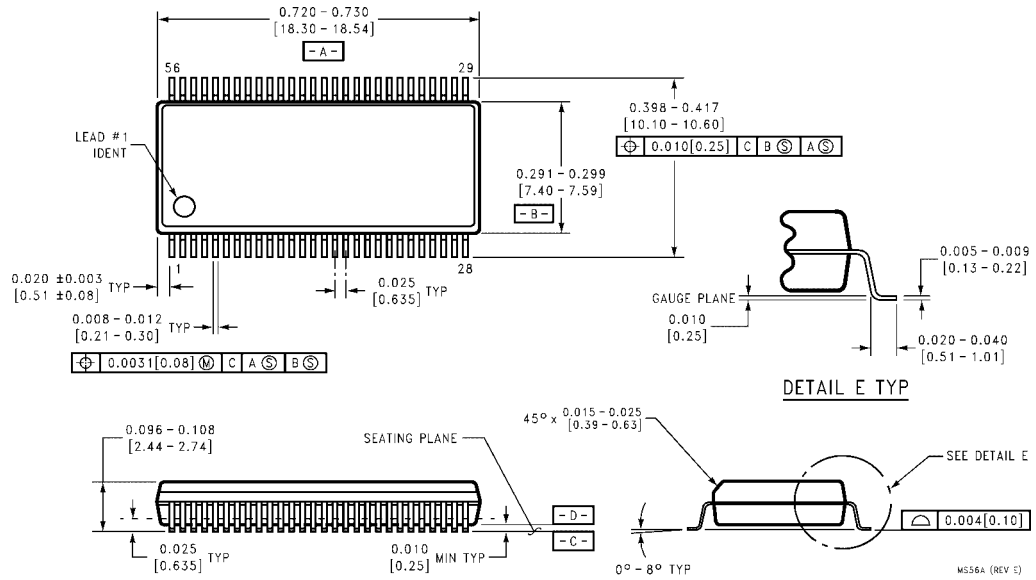


- NOTES:
- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
  - B. ALL DIMENSIONS IN MILLIMETERS
  - C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
  - D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide**  
**Package Number BGA54A**  
**Preliminary**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

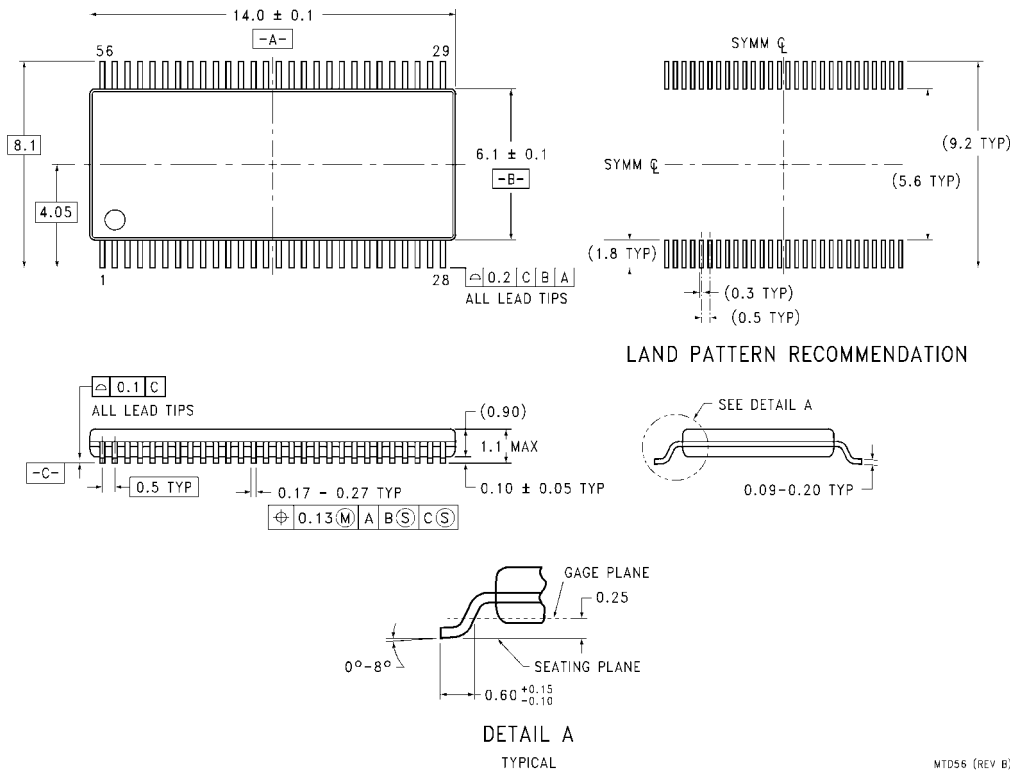


**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS56A**

MS56A (REV E)



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)