Octal inverting buffer (3–State) 74ABT240

FEATURES

- Octal bus interface
- 3–State buffers
- Output capability: +64mA/–32mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT240 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT240 device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3–State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF; V_{CC} = 5V	3.5	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Ouputs disabled; V_{CC} =5.5V	500	nA

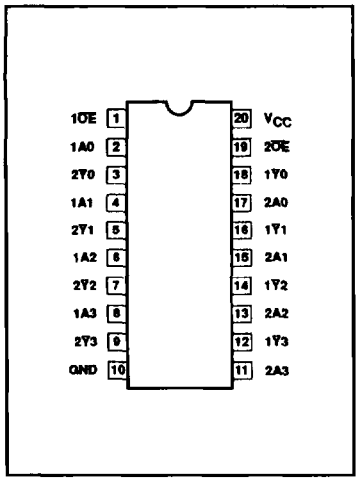
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20–pin plastic DIP	–40°C to +85°C	74ABT240N
20–pin plastic SOL	–40°C to +85°C	74ABT240D

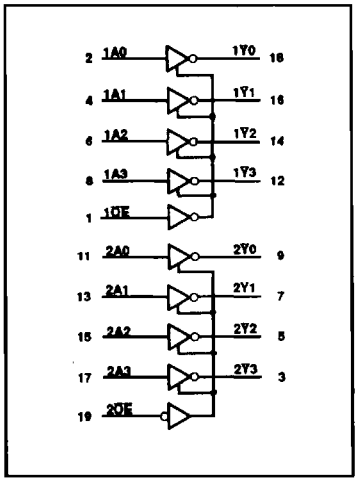
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	$1\overline{Y}0$ – $1\overline{Y}3$	Data outputs
9, 7, 5, 3	$2\overline{Y}0$ – $2\overline{Y}3$	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

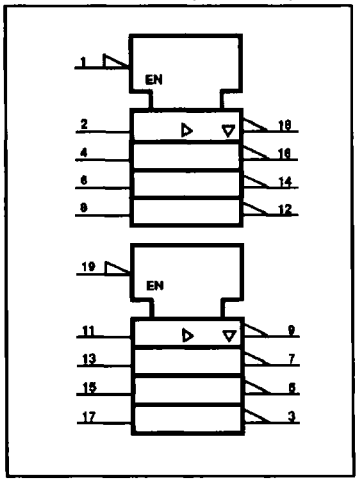
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	1Yn	1Yn
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		–32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	operating free–air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3–State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3–State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_O	Short–circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		0.5	mA
		Outputs 3–State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3–State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		0.5	mA

NOTES:
1 Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2 This is the increase in supply current for each input at 3.4V.