



High Speed CMOS 16-Bit Latches

QS74FCT16373T

QS74FCT162373T

FEATURES/BENEFITS

- 16-bit Function compatible to the 74F373 and 74FCT373
- CMOS power levels: <7.5 mW static
- Available in VSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 16373T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, and C speed grades; 4.1ns tPD for C
- I_{OL} = 64 mA Com., 48 mA Mil.

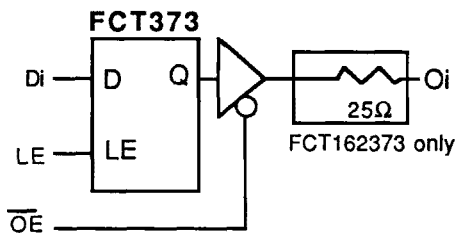
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- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A, and C speed grades; 4.1 ns tPD for C
- I_{OL} = 12mA Com.

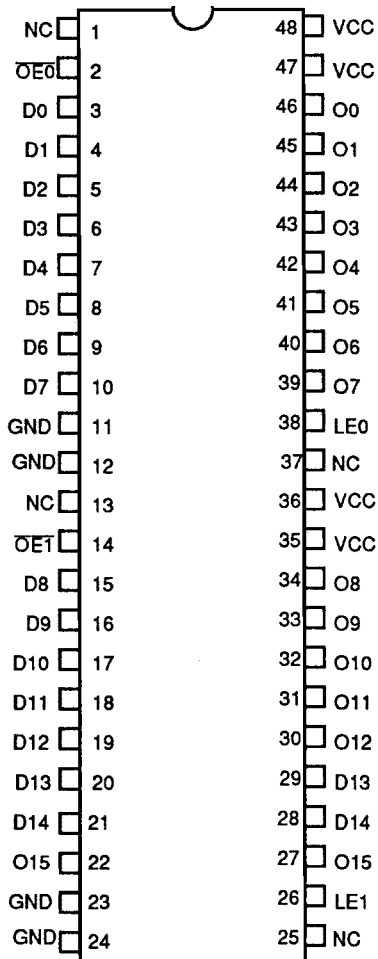
DESCRIPTION

The QSFCT16373AT/CT and QSFCT162373AT/CT are 16-bit non-inverting transceivers that have three-state outputs which are useful for bus-oriented applications. The Transmit/Receive (T/R) input determines the direction of data flow, either from A to B or B to A, and the Output Enable (OE) input enables the selected port for output. The FCT162373AT/CT are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. All inputs have clamp diode for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PINOUPS



QSFCT16373T Advanced Information

PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
LE	I/O	Latch Enable
\overline{OE}	I/O	Output Enable

FUNCTION TABLE

Inputs			Internal Q Value	Outputs Oi	Function
\overline{OE}	LE	Di			
H	X	X	X	Z	Disable Outputs
L	X	X	H	H	Enable Outputs
L	X	X	L	L	
X	H	L	L	X	Pass Input Data
X	H	H	H	X	
X	L	X	Q	X	Hold Prior Data

H=High, L=Low, Hi-Z=High Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....	-0.5V to +7.0V
DC Output Voltage V_O	-0.5V to 7.0V
DC Input Voltage V_I	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns).....	-3.0V
DC Input Diode Current with $V_I < 0$	-20 mA
DC Output Diode Current with $V_O < 0$	-50 mA
DC Output Current Max. sink current/pin.....	120 mA
Maximum Power Dissipation.....	0.5 watts
T_{STG} Storage Temperature.....	-65° to +165°C

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CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$

Pins	VSOP	Unit
2,14,34,46	4	pF
-----	6	pF
3-10,15-22, 26-33, 38-45	8	pF

Note: Capacitance is characterized but not tested

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V}\pm 5\%$

Military $T_A=-55^{\circ}\text{C}$ to 125°C , $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit	
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts	
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8		
ΔV_t	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-		
$ I_{ih} $ $ I_{il} $	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	μA	
$ I_{oz} $	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}, 0 \leq V_{in} \leq V_{CC}$		-	-	5		
Ios	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}, V_o = \text{GND} (2,3)$		-60	-	-255	mA	
Ior	Current Drive FCT2XXX (25 Ω)	$V_{CC} = \text{Min}, V_o = 2.0\text{V}$		50	-	-	mA	
Vic	Input Clamp Voltage	$V_{CC} = \text{MIN}, I_{in} = 18 \text{ mA} (3)$		-	-0.7	-1.2	Volts	
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	loh = 12 mA (MIL)	2.4	-	-	Volts	
			loh = 15 mA (COM)	2.4	-	-		
Vol	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	lol = 48 mA (MIL)	-	-	0.55		
			lol = 64 mA (COM)	-	-	0.55		
	Output LOW Voltage FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	lol = 12 mA (MIL)	-	-	0.50		
			lol = 12 mA (COM)	-	-	0.50		
Rout	Output Resistance FCT2XXX (25 Ω)	$V_{CC} = \text{MIN}$	lol = 12 mA (MIL)	-	25	-		Ω
			lol = 12 mA (COM)	20	28	40		

Notes:

1. Typical values indicate $V_{CC}=5.0\text{V}$ and $T_A=25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I _{cc}	Quiescent Power Supply Current	V _{cc} = MAX, freq = 0 0V ≤ V _{in} ≤ 0.2V or V _{cc} - 0.2V ≤ V _{in} ≤ V _{cc}	-	3.0	mA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = MAX, V _{in} = 3.4 V, freq = 0 (2)	-	2.0	
Q _{ccd}	Supply Current per input per mHz	V _{cc} = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V _{cc} (3,4)	-	0.25	mA/ MHz

For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
Per TTL driven input (V_i=3.4V)

For flipflops Q_{ccd} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested. I_c can be computed using the above parameters as explained in the Technical Overview section.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: Ta = 0 °C to 70 °C, Vcc = 5.0V ±5% Military: Ta = -55 °C to +125 °C, Vcc = 5.0V ±10%
 Cload = 50 pF, Rload = 500Ω unless otherwise noted.

Symbol	Description	Notes (1)	16373A 162373A		16373C, 162373C		Unit
			Min	Max	Min	Max	
t PHL t PLH	Propagation Delay Data to Oi, 373	COM	1.5	5.2	1.5	4.7	ns
		MIL	1.5	5.6			
	Propagation Delay Data to Oi, 2373	COM	1.5	5.2	1.5	4.7	
		MIL	1.5	5.6			
t PHLE t PLHE	Propagation Delay LE high to Oi, 373	COM	2	8.5	2	6.9	
		MIL	2	9.8			
	Propagation Delay LE high to Oi, 2373	COM	2	8.5	2	6.9	
		MIL	2	9.8			
t PZH t PZL	Output Enable Time OE to Yi, 373	COM	1.5	6.5	1.5	5.5	
		MIL	1.5	7.5			
	Output Enable Time OE to Yi, 2373	COM	1.5	6.5	1.5	6.2	
		MIL	1.5	7.5			
t PHZ t PLZ	Output Disable Time OE to Yi	COM	2	1.5	5.5	1.5	5.0
		MIL	2	1.5	6.5		
t S	Data Setup Time Di to LE hi to low	COM	2		2		
		MIL	2				
t H	Data Hold Time Di to LE hi to low	COM	1.5		1.5		
		MIL	1.5				
t W	LE Pulse Width HIGH or LOW	COM	2	5	4		
		MIL	2	6			

Notes:

1. Minimum propagation delay values are guaranteed but not tested.
2. This parameter is guaranteed but not tested.