



# High Speed CMOS Dual 4 Input Multiplexers

QS54/74FCT153T  
QS54/74FCT253T

QS54/74FCT2153T  
QS54/74FCT2253T

## FEATURES/BENEFITS

- Pin and function compatible to the 74F153/253 74FCT153/253 and 74FCT153T/253T
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

### FCT-T 153T, 253T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std. and A speed grades with 4.5 ns  $t_{PD}$  for C
- $I_{OL} = 48$  mA Com., 32 mA Mil.

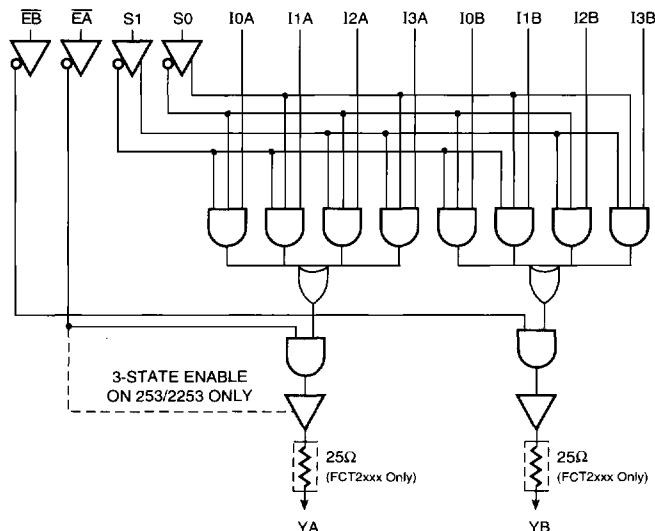
### FCT-T 2153T, 2253T

- Built-in  $25\Omega$  series resistor outputs reduce reflection and other system noise
- Std and A speed grades with 5.2 ns  $t_{PD}$  for A
- $I_{OL} = 12$  mA Com.

## DESCRIPTION

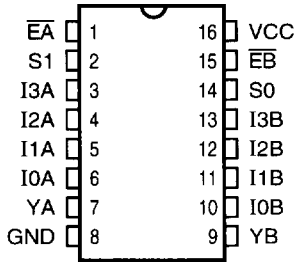
The QSFCT153T and QSFCT253T are high-speed CMOS TTL-compatible dual 4-input multiplexers. The 153T has 3-state outputs; the 253T has 3-state outputs. The QSFCT2153T and QSFCT2253T are  $25\Omega$  resistor output versions useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001). Outputs will not load an active bus when  $V_{CC}$  is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM

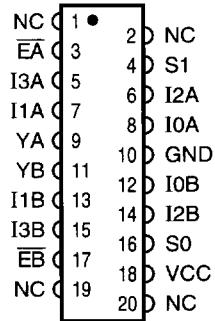


**PIN CONFIGURATIONS (All Pins Top View)**

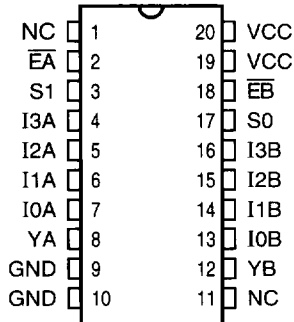
**PDIP, SOIC, QSOP**



**ZIP**



**HQSOP**



**Note:**

Available in both 150 mil wide SOIC (package code S1) and 300 mil wide SOIC (package code S0).

**PIN DESCRIPTION**

Name	I/O	Description
I7-I0	I	Data In
S1-S0	I	Select
EA, EB	I	Enable
YA, YB	O	Data Out

**FUNCTION TABLE**

Enable		Select		153, 2153		253, 2253		Function
EA	EB	S1	S0	YA	YB	YA	YB	
H	X	X	X	L	X	HI-Z	Z	Disable A
X	H	X	X	X	L	X	HI-Z	Disable B
L	L	L	L	I0A	I0B	I0A	I0B	S1-0 = 0
L	L	L	H	I1A	I1B	I1A	I1B	S1-0 = 1
L	L	H	L	I2A	I2B	I2A	I2B	S1-0 = 2
L	L	H	H	I3A	I3B	I3A	I3B	S1-0 = 3

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20 mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-6, 10-15	4	4	5	7	pF
7, 9	6	6	7	9	pF
—	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , $\text{freq} = 0$ <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ , Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}$ <sup>(3,4)</sup>	—	0.25	mA/MHz

**Notes:**

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
- For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

**QSFCT153T, 253T, 2153T, 2253T**

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)(253, 2253)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current FCTXXX	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$I_{OR}$	Current Drive FCT2XXX	$V_{CC} = \text{Max.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	— —	— —	V
$V_{OL}$	Output LOW Voltage FCTXXX	$V_{CC} = \text{Min.}, I_{OL} = 32 \text{ mA (MIL)}$ $I_{OL} = 48 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
$V_{OL}$	Output LOW Voltage FCT2XXX (25 $\Omega$ )	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
$R_{OUT}$	Output Resistance FCT2XXX (25 $\Omega$ )	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— 20	25 28	— 40	$\Omega$

**3**

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**QSFCT153T, 253T, 2153T, 2253T**

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>		153 253 2153 2253		153A 253A 2153A 2253A		153C 253C 2153C 2253C		Unit
			Min	Max	Min	Max	Min	Max	
t <sub>IY</sub>	Propagation Delay In to Y, 153/253	Com	1.5	7	1.5	5.2	1.5	4.5	ns
		Mil	1.5	8	1.5	5.8			
t <sub>IY</sub>	Propagation Delay In to Y, 2153/2253	Com	1.5	7	1.5	5.2	1.5	4.5	ns
		Mil	1.5	8	1.5	5.8			
t <sub>SY</sub>	Propagation Delay S <sub>n</sub> to Y, 153/253	Com	1.5	9	1.5	6.6	1.5	5.6	ns
		Mil	1.5	9.5	1.5	7.4			
t <sub>SY</sub>	Propagation Delay S <sub>n</sub> to Y, 2153/2253	Com	1.5	9	1.5	6.6	1.5	5.6	ns
		Mil	1.5	9.5	1.5	7.4			
t <sub>OE<sub>H</sub></sub> t <sub>OE<sub>L</sub></sub>	Output Enable Time $\bar{E}$ to Y <sub>i</sub> , 153	Com	1.5	7	1.5	5.2	1.5	4.8	ns
		Mil	1.5	8	1.5	5.8			
t <sub>OE<sub>H</sub></sub> t <sub>OE<sub>L</sub></sub>	Output Enable Time $\bar{E}$ to Y <sub>i</sub> , 2153	Com	1.5	7	1.5	5.2	1.5	4.8	ns
		Mil	1.5	8	1.5	5.8			
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\bar{E}$ to Y <sub>i</sub> , 253	Com	1.5	9	1.5	6.0	1.5	5.0	ns
		Mil	1.5	10	1.5	6.4			
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\bar{E}$ to Y <sub>i</sub> , 2253	Com	1.5	9	1.5	6.0	1.5	5.0	ns
		Mil	1.5	10	1.5	6.4			
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time <sup>(2)</sup> $\bar{E}$ to Y <sub>i</sub> , 253/2253	Com	1.5	7	1.5	6	1.5	5.0	ns
		Mil	1.5	7	1.5	6.3			

**Notes:**

1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.