

M02040

3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

Data Sheet

3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

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Advance Information

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FEATURES

- ❑ Operates with a 3.3 or 5V supply
- ❑ 4 mV input sensitivity at 2.5 Gbps
- ❑ PECL outputs
- ❑ Average Receive power monitor output (RSSI_{AVG})
- ❑ Peak-to-peak Receive power monitor output (RSSI_{PP})
- ❑ On-chip DC offset cancellation circuit
Offset cancellation circuit can be disabled for Burst mode applications
- ❑ Low power (< 80 mW at 3.3V)
- ❑ Output Jam function
- ❑ 16-pin 3x3 mm QFN package

APPLICATIONS

- ❑ 2.5 Gbps STM-16/OC-48 SDH/SONET
- ❑ 1.06 and 2.12 Gbps Fibre Channel
- ❑ 1.25 Gbps Ethernet
- ❑ 2.67 Gbps SDH/SONET with FEC

DESCRIPTION

The M02040 is an integrated high-gain limiting amplifier. Featuring PECL outputs, the M02040 is useable in applications to 2.5 Gbps. Full output swing is achieved even at minimum input sensitivity. The M02040 can operate with a 3.3V or 5V supply.

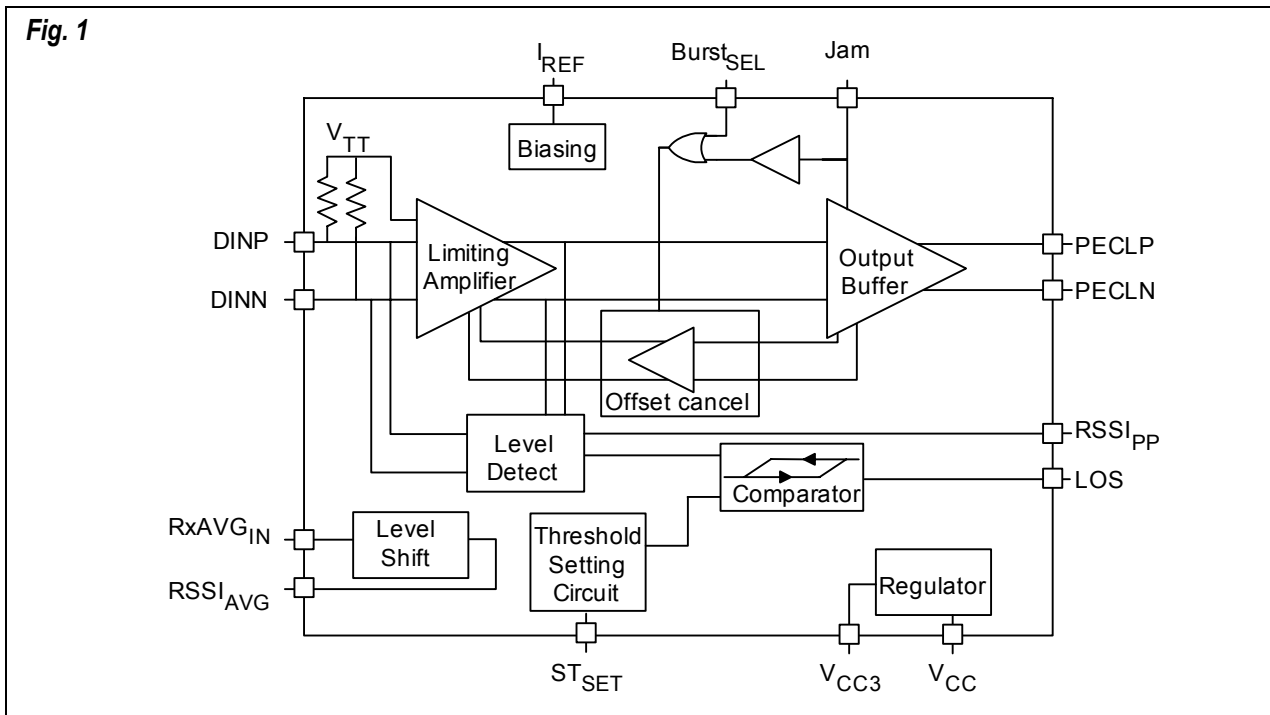
Burst select is supported for PON applications requiring instantaneous output response.

The M02040 also includes two analog RSSI outputs proportional to either the average or peak to peak input signal and a programmable signal-level detector allowing the user to set thresholds at which the logic outputs are enabled.

TABLE 1 ORDERING INFORMATION

Part Number	Pin Package
M02040	M02040 in QFN16 package
M02040-EVM	Evaluation board with M02040

TOP LEVEL DIAGRAM



3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

TABLE 2 _____ PIN DESCRIPTIONS

QFN Pin#	Name	Function
1	GND	Ground.
2	V _{CC}	Power supply. Connect to either +5V or +3.3V.
3	PECLN	Inverting data output (PECL).
4	PECLP	Non-inverting data output (PECL).
5	I _{REF}	Internal reference current. Must be connected to ground through a 12.1kΩ 1% resistor.
6	ST _{SET}	Loss of signal threshold setting input. Connect a 1% resistor between this pin and V _{CC3} to set loss of signal threshold.
7	V _{CC3}	Power supply input for 3.3V applications or the output of the internally regulated 3.3V voltage when V _{CC} = 5V. Connect directly to supply for 3.3V applications (internal regulator not in use). Do not connect to power supply if V _{CC} = 5V.
8	BURST _{SEL}	Burst-mode select. When high, the DC servo circuit is disabled, allowing the limiting amplifier to be used with burst-mode data. Also useful for operating data path with low-speed or DC signals. When low or floating, DC servo is enabled. Internal 80kΩ resistor to ground.
9	DINP	Non-inverting data input. Internally terminated with 50Ω to V _{TT} .
10	DINN	Inverting data input. Internally terminated with 50Ω to V _{TT} .
11	GND	Ground.
12	RxAVG _{IN}	Average power monitor input. Connect to monitor output of TIAs that produce a current (sink) mirror replica of the photodiode current. Leave floating if not used.
13	JAM	Output disable. When high, data outputs are disabled (with non-inverting output held high and inverting output held low). Connect to LOS output to disable outputs with loss of signal. Outputs are enabled when JAM is low or floating. Internal 150kΩ resistor to ground.
14	LOS	Loss of signal output. Goes high when input signal falls below threshold set by ST _{SET} . Open collector TTL with internal 80kΩ pull-up resistor to V _{CC} .
15	RSSI _{AVG}	Receiver average input power monitor. Provides a current source mirror of the current at RxAVG _{IN} . Connect a resistor to ground to set the full scale voltage to the desired level at maximum average input power.
16	RSSI _{PP}	Receiver peak-to-peak input voltage monitor. Provides a DC voltage (ground referenced) proportional to the peak-to-peak input voltage swing.
17	Center Pad	Ground. Must be connected to ground for proper operation.

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TABLE 3 _____ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V _{CC}	Power supply voltage (V _{CC} -GND)	-0.5 to +6V	V
T _{STG}	Storage temperature	-65 to +150	°C
PECLP, PECLN	PECL Output pins voltage	V _{CC} - 0.4 to V _{CC} + 0.4	V
DINP - DINN	Data input pins differential voltage	0.80	V
DINP, DINN	Data input pins voltage meeting DINP - DINN requirement	GND to V _{CC3} + 0.4	V
ST _{SET}	Signal detect threshold setting pin voltage	GND to V _{CC} + 0.4	V
JAM	Output enable pin voltage	GND to V _{CC} + 0.4	V
LOS	Status Output pins voltage	GND to V _{CC} + 0.4	V
Burst_Sel	Burst Select input pin voltage	GND to V _{CC} + 0.4	V
I _{REF}	Current into Reference input	+ 0 to -120	µA
I(RSSI _{AVG})	Current into RSSI _{avg} input	+ 0 to -3	mA
RSSI _{PP}	RSSI _{PP} pin voltage	GND to +3.6	V
I(LOS)	Current into Loss of Signal pin	+1500 to -100	µA

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Note: The package bottom must be adequately grounded to ensure correct thermal and electrical performance, and it is recommended that vias are inserted through to a lower ground plane.

TABLE 4 _____ RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Units
Power supply: (V _{CC} -GND) (apply no potential to V _{CC3}) or (V _{CC3} -GND) (connect V _{CC} to same potential as V _{CC3})	+5V ± 7.5% or +3.3V ± 7.5%	V
Junction temperature	-40 to +110	°C
Operating ambient	-40 to +85	°C

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TABLE 5 _____ DC CHARACTERISTICS

$V_{CC} = +3.3V \pm 7.5\%$ or $+5V \pm 7.5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.
 Typical specifications are for $V_{CC} = 3.3V$, $T_A = 25^{\circ}C$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	Outputs terminated into 50Ω to V_{CC} (includes PECL load)		52		mA
$V_{OUTL_{pecl}}$	PECL Output Low Voltage (PECLP, PECLN)	Single ended; 50Ω load to $V_{CC}-2V$	$V_{CC}-1.81$	$V_{CC}-1.71$	$V_{CC}-1.62$	V
$V_{OUTH_{pecl}}$	PECL Output High Voltage (PECLP, PECLN)	Single ended; 50Ω load to $V_{CC}-2V$	$V_{CC}-1.025$	$V_{CC}-0.952$	$V_{CC}-0.88$	V
	Differential Input Resistance	Measured between DINP and DINN	85	100	115	Ω
	Differential Output Resistance	Measured between CMLP and CMLN	170	200	230	Ω
	LOS Output High Voltage	External 4.7-10k Ω pull up to V_{CC}	2.4	V_{CC}		V
	LOS Output Low Voltage	External 4.7-10k Ω pull up to V_{CC}	0		0.4	V
	Logic Input High Voltage JAM, BURST _{SEL}		2.7		5.5	V
	Logic Input Low Voltage JAM, BURST _{SEL}				0.8	V

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TABLE 6 AC CHARACTERISTICS

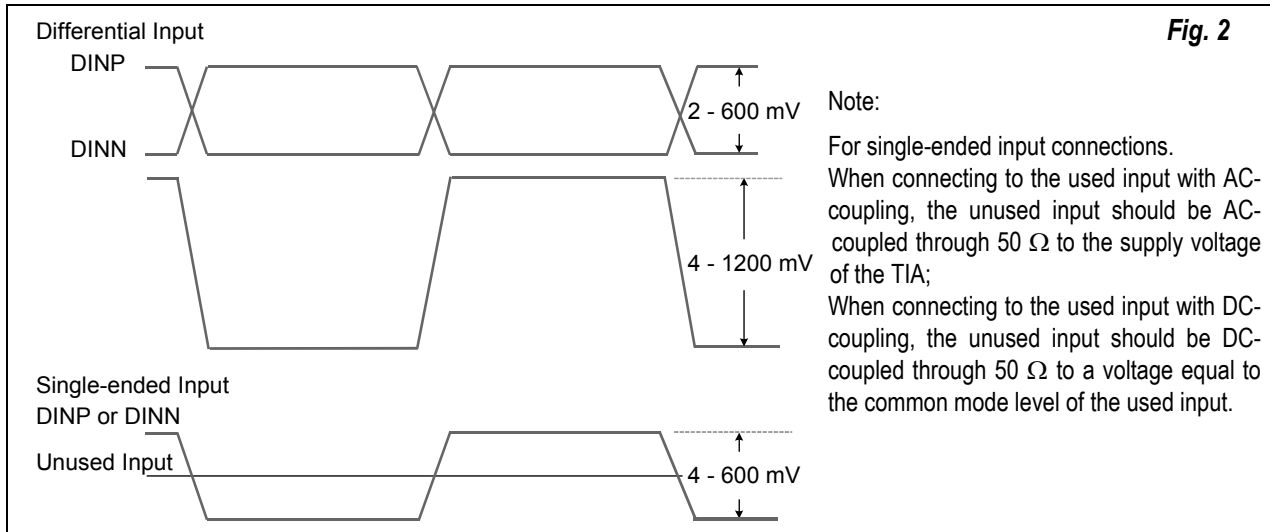
V_{CC} = +3.3V ± 7.5% or +5V ± 7.5%, T_A = -40°C to +85°C, input bit rate = 2.5 Gbps 2²³-1 PRBS unless otherwise noted. Typical specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IN(MIN)}	Differential Input Sensitivity	2.5 Gbps, BER < 10 ⁻¹²			4	mV
		3.3 Gbps, BER < 10 ⁻¹²		5		mV
		4.3 Gbps, BER < 10 ⁻¹²		6		mV
V _{I(MAX)}	Input Overload	BER < 10 ⁻¹² , differential input 2.5 Gbps	1200			mV
		BER < 10 ⁻¹² , single-ended input, 2.5 Gbps	600			mV
v _n	RMS Input Referred Noise			185		μV _{RMS}
V _{SD}	Signal Detect Programmable Range	Differential inputs	4		100	mV
HYS	Signal Detect Hysteresis	(electrical); signal detect level set to 20 mV p-p	2	4	6	dB
RSS _{lpp}	Peak-to-peak received signal strength indicator range		4		100	mV
RSS _{lave}	Average received signal strength indicator range	± 15% accuracy ± 20% accuracy	5 0.5		500 2	μA mA
BW _{LF}	Small-Signal -3dB Low Frequency Cutoff	Excluding AC coupling capacitors		25		kHz
DJ	Deterministic Jitter	K28.5 pattern at 2.125 Gbps			25	ps
RJ	Random Jitter	10mV _{PP} input		3		ps _{RMS}
t _r / t _f	Data Output Rise and Fall Times	20% to 80%; outputs terminated into 50Ω; 10mV _{PP} input		185	300	ps
T _{LOS_ON}	Time from LOS state until LOS output is asserted	LOS assert time after 1Vp-p input signal is turned off; signal detect level set to 10mV			100	μs
T _{LOS_OFF}	Time from non-LOS state until LOS is deasserted	LOS deassert time after input crosses signal detect level; signal detect set to 10mV with applied input signal of 20mV _{PP}			100	μs

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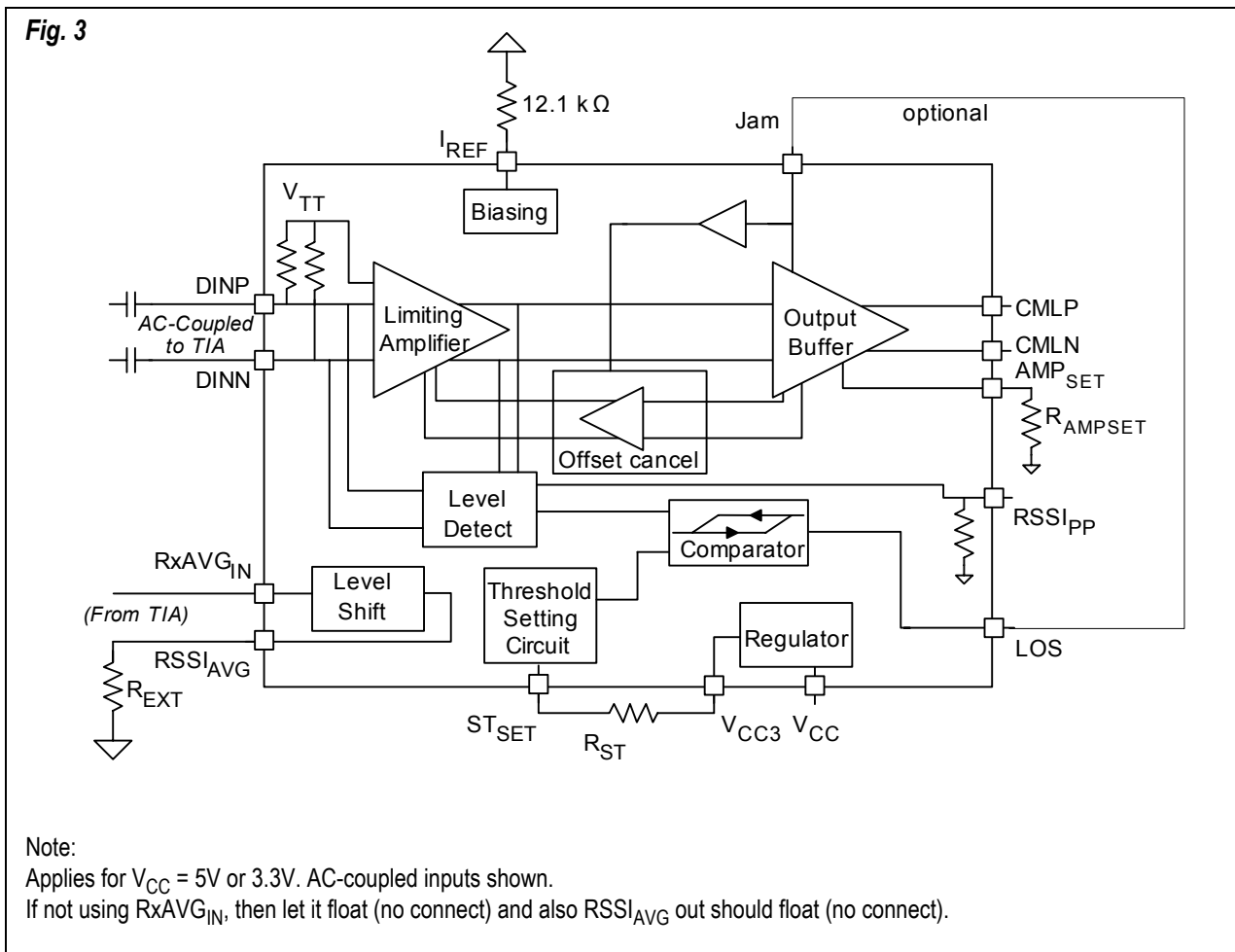
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DATA INPUT REQUIREMENTS



Advance Information

TYPICAL APPLICATIONS CIRCUIT



3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

FUNCTIONAL DESCRIPTION

Overview

The M02040 is a high-gain limiting amplifier for applications up to 2.5 Gbps and incorporates a limiting amplifier, an input signal level detection circuit and also a fully integrated DC-offset cancellation loop that does not require any external components. The M02040 features PECL data outputs.

The M02040 provides the user with the flexibility to set the signal detect threshold. Optional output buffer disable (squelch/jam) can be implemented using the JAM input.

Inputs (Fig. 4)

The data inputs are internally connected to V_{TT} via $50\ \Omega$ resistors, and generally need to be AC coupled. Referring to Fig. 4, the nominal V_{TT} voltage is 2.85V because of the internal resistor divider to V_{CC3} , which means this is the DC potential on the data inputs. See the applications information section for further details on choosing the AC-coupling capacitor.

DC Offset Compensation

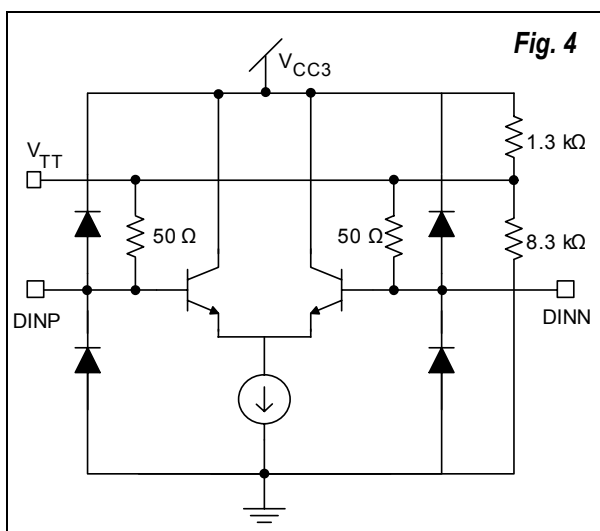
The M02040 contain an internal DC autozero circuit that can remove the effect of DC offsets without using external components. This circuit is configured such that the feedback is effective only at frequencies well below the lowest frequency of interest. The low frequency cut off is typically 25 kHz.

Data Outputs (Fig. 5)

The M02040 features 100k/300k PECL compliant outputs as shown in Fig. 5. The outputs may be terminated using any standard AC or DC-coupling PECL termination technique. AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drive and compatibility with non-PECL interfaces.

Advance Information

CML DATA INPUTS



3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

FUNCTIONAL DESCRIPTION

PECL DATA OUTPUTS

Advance Information

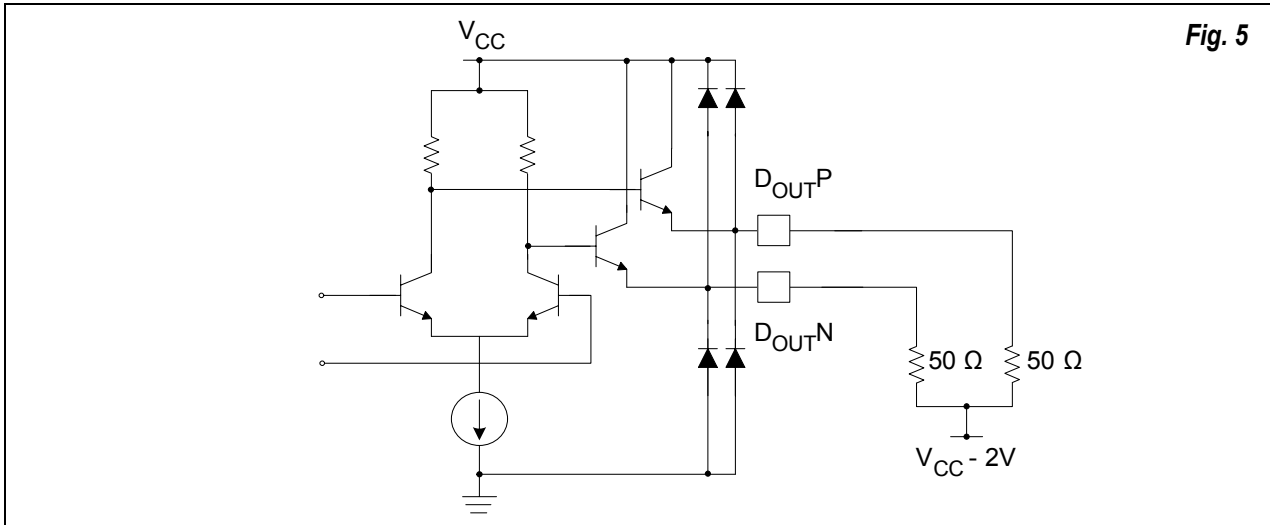


Fig. 5

Loss of Signal (LOS) (Fig. 6 and Fig. 7)

The M02040 features input signal level detection over an extended range. Using an external resistor, R_{ST} , between pin ST_{SET} and V_{CC3} (Fig. 7) the user can program the input signal threshold. The signal detect status is indicated on the LOS output pin shown in Fig. 6. The LOS signal is active when the signal is below the threshold value. The signal detection circuitry has the equivalent of 4dB (typical) electrical hysteresis.

R_{ST} establishes a threshold voltage at the ST_{SET} pin as shown in Fig. 7. Internally, the input signal level is monitored by the Level Detector (which also outputs the $RSSI_{PP}$ voltage). As described in the $RSSI_{PP}$ section, this voltage is proportional to the input signal peak to peak value. The voltage at ST_{SET} is internally compared to the signal level from the Level Detector. When the Level Detect voltage is less than $V_{(STSET)}$, LOS is asserted and will stay asserted until the input signal level increases by a predefined amount of hysteresis. When the input level increases by more than this hysteresis above $V_{(STSET)}$, LOS is deasserted. See the applications information section for the selection of R_{ST} .

Note that ST_{SET} can be left open if the loss of signal detector function is not required. In this case LOS would be low.

LOS OUTPUT

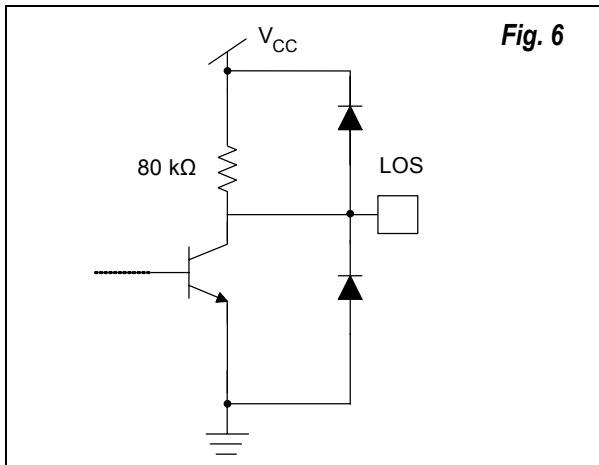
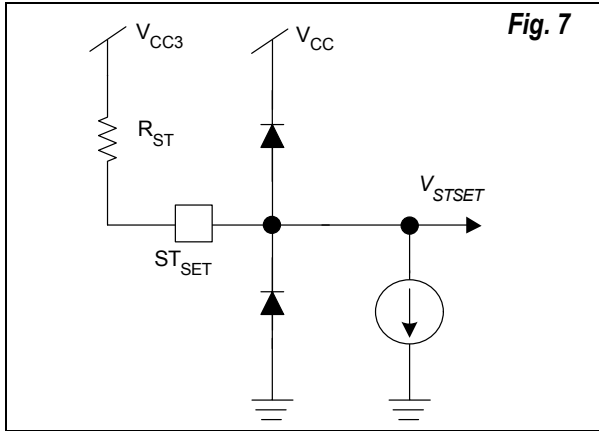


Fig. 6

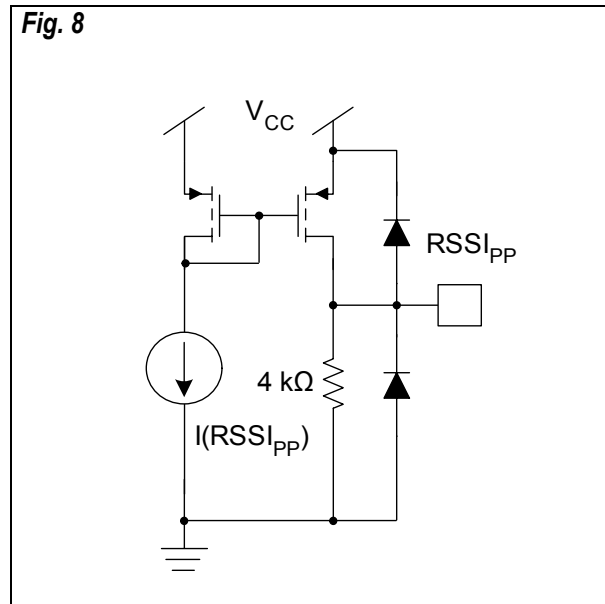
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FUNCTIONAL DESCRIPTION

STSET INPUT



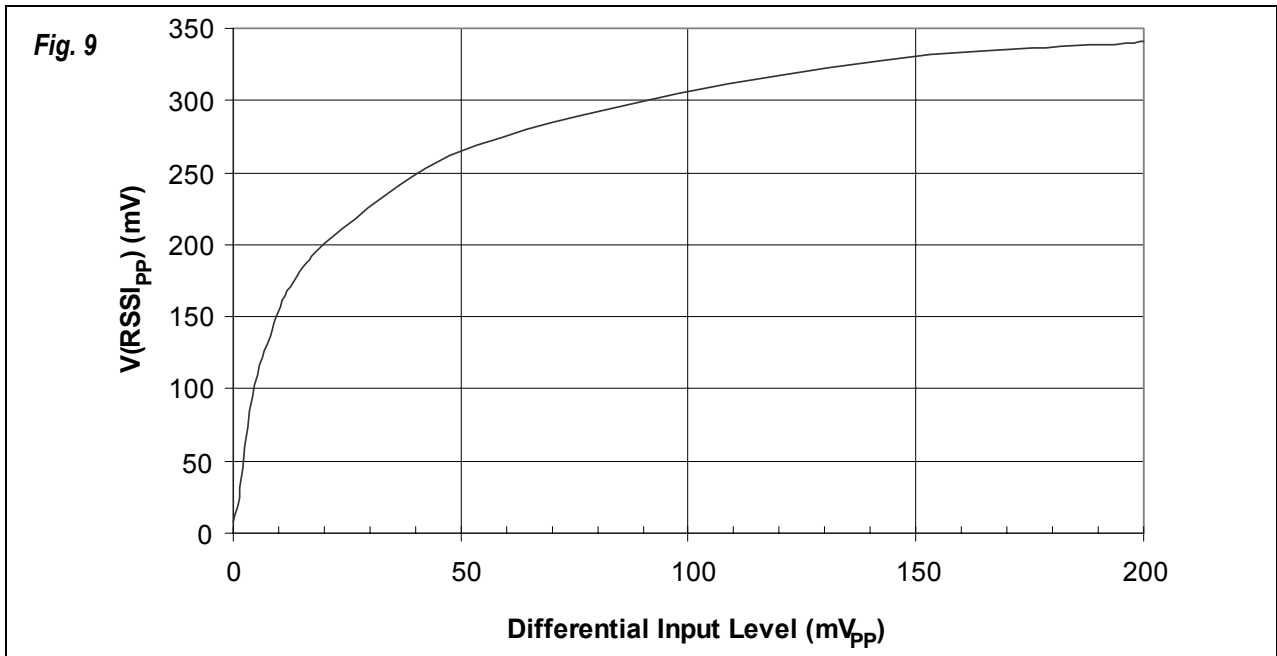
RSSI_{PP} OUTPUT



Peak to Peak Received Signal Strength Indicator (RSSI_{PP}) (Fig 8).

The RSSI_{PP} output voltage is proportional to the peak to peak level of the input signal. It is not necessary to connect an external capacitor to this output. Internally, the RSSI voltage is compared with a user selectable reference to determine loss of signal as described in the previous section.

RSSI_{PP} TRANSFER FUNCTION

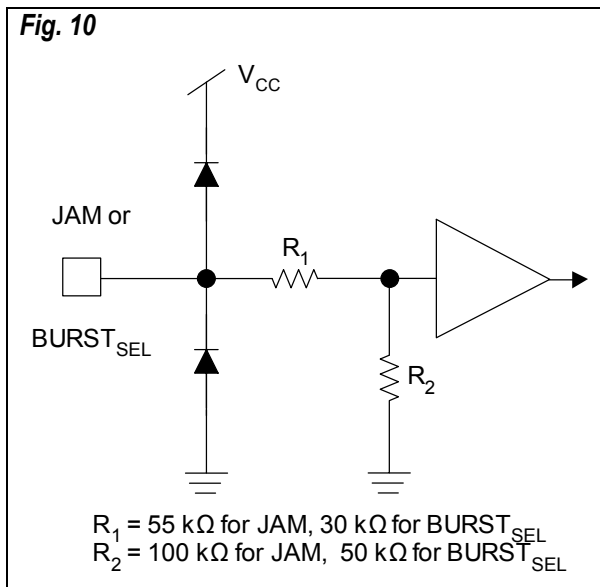


JAM Function (Fig. 10)

When asserted, the active high power down (JAM) pin forces the outputs to a logic “one” state. This ensures that no data is propagated through the system. The loss of signal detection circuit can be used to automatically force the data outputs to a high state when the input signal falls below the threshold. The function is normally used to allow data to propagate only when the signal is above the user’s bit-error-rate requirement. It therefore inhibits the data outputs toggling due to noise when there is no signal present (“squelch”).

In order to implement this function, LOS should be connected to the JAM pin shown in Fig. 10, thus forcing the data outputs to a logic “one” state when the signal falls below the threshold.

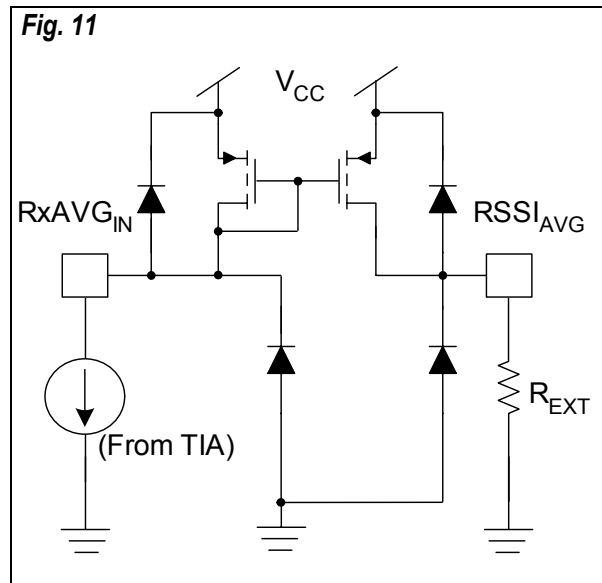
JAM & BURST_{SEL} INPUT



Average Received Signal Strength Indicator (RSSI_{AVG}) (Fig. 11)

The RSSI_{AVG} output current is a mirrored version of the RxAVG_{IN} current from compatible TIAs. It sources rather than sinks the current making it compatible with DDMI type interfaces.

RSSI_{AVG} OUTPUT



Voltage Regulation

The M02040 contain an on-chip voltage regulator to allow both 5V and 3.3V operation. When used at 5V, the on-chip regulator is enabled and the digital inputs and outputs are compatible with TTL 5V logic levels.

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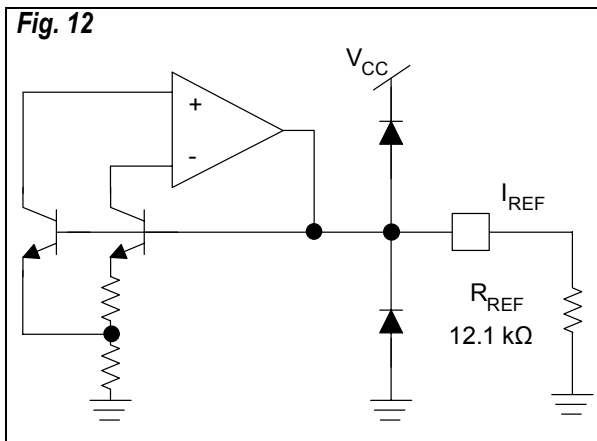
3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

APPLICATIONS INFORMATION

Reference Current Generation (Fig. 12)

The M02040 contain an accurate on-chip bias circuit that requires an external 12.1 kΩ 1% resistor, R_{REF}, from pin I_{REF} to ground to define an on-chip reference current.

REFERENCE CURRENT CONNECTION



Connecting V_{CC} and V_{CC3}

For 5V operation, the V_{CC} pin is connected to an appropriate 5V ± 7.5% supply. No potential should be applied to the V_{CC3} pin. The only connection to V_{CC3} should be R_{ST} as shown in Fig. 7.

When V_{CC} = 5V all logic outputs and the data outputs are 5V compatible while the CML data inputs are still referenced to 3.3V from the internal regulator (see Fig. 4). For low power operation, V_{CC} and V_{CC3} should be connected to an appropriate 3.3V ± 7.5% supply. In this case all I/Os are 3.3V compatible.

Choosing an Input AC-Coupling Capacitor

When AC-coupling the input the coupling capacitor should be of sufficient value to pass the lowest frequencies of interest, bearing in mind the number of consecutive identical bits, and the input resistance of the part. For SONET data, a good rule of thumb is to chose a coupling capacitor that has a cut-off frequency less than 1/(10,000) of the input data rate. For example, for 2.5 Gbps data, the coupling capacitor should be chosen as:

$$f_{CUTOFF} \leq (2.5 \times 10^9 / 10 \times 10^3) = 250 \times 10^3$$

The -3 dB cutoff frequency of the low pass filter at the 50 Ω input is found as:

$$f_{3dB} = 1 / (2 * \pi * 50 \Omega * C_{AC})$$

so solving for C where $f_{3dB} = f_{CUTOFF}$

$$C_{AC} = 1 / (2 * \pi * 50 \Omega * f_{CUTOFF}) \tag{EQ.1}$$

and in this case the minimum capacitor is 12 nF.

For Ethernet or Fibre Channel, there are less consecutive bits in the data, and the recommended cut-off frequency is 1/(1,000) of the input data rate. This results in a minimum capacitor of 1.5 nF for 2.125 Gbps Fibre Channel.

Multirate applications down to 155 Mbps

In this case, the input coupling capacitor needs to be large enough to pass 15 kHz (155x10⁶/10,000) which results in a capacitor value of 0.2 μF. However, because this low pass frequency is close to the 25 kHz low pass frequency of the internal DC servo loop, it is preferable to use a larger input coupling capacitor such as 1 μF which provides an input cutoff frequency of 3.1 kHz. This separates the two poles sufficiently to allow them to be considered independent. This capacitor should also have a 10 nF capacitor in parallel to pass the higher frequency data (in the multirate application) without distortion.

In all cases, a high quality coupling capacitor should be used as to pass the high frequency content of the input data stream.

Using Burst Selection

When the BURST_{SEL} pin (shown in Fig. 11) is tied high, the M02040 disables the internal servo loop which allows the device to pass signals with DC content resulting in much quicker response to burst-mode data. However, there is no correction for limit amp offset when the servo loop is disabled which results in degraded sensitivity and increased duty cycle distortion. For normal operation the BURST_{SEL} pin should be tied low or left floating.

Advance Information

3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

APPLICATIONS INFORMATION

Advance Information

Using $RSSI_{AVG}$

As shown in the typical applications circuit (Fig. 3), when interfacing to a TIA that features a “MON” output such as the M02010 or M02013, the M02040 can reference the current sunk into the TIA “MON” output and produce a proportional current at the 2040 $RSSI_{AVG}$ output. The current is sourced into resistor R_{EXT} to ground creating a voltage suitable for DDMI applications. R_{EXT} should be chosen as:

$$R_{EXT} = 1/(\text{maximum current into } RSSI_{AVG}) \quad \text{EQ.2}$$

This keeps the voltage at $RSSI_{AVG}$ between 0 and 1 V.

Setting the Signal Detect Level

Using Fig. 13, the value for R_{ST} is chosen to set the LOS threshold at the desired value. The resulting hysteresis is also shown in Fig. 13.

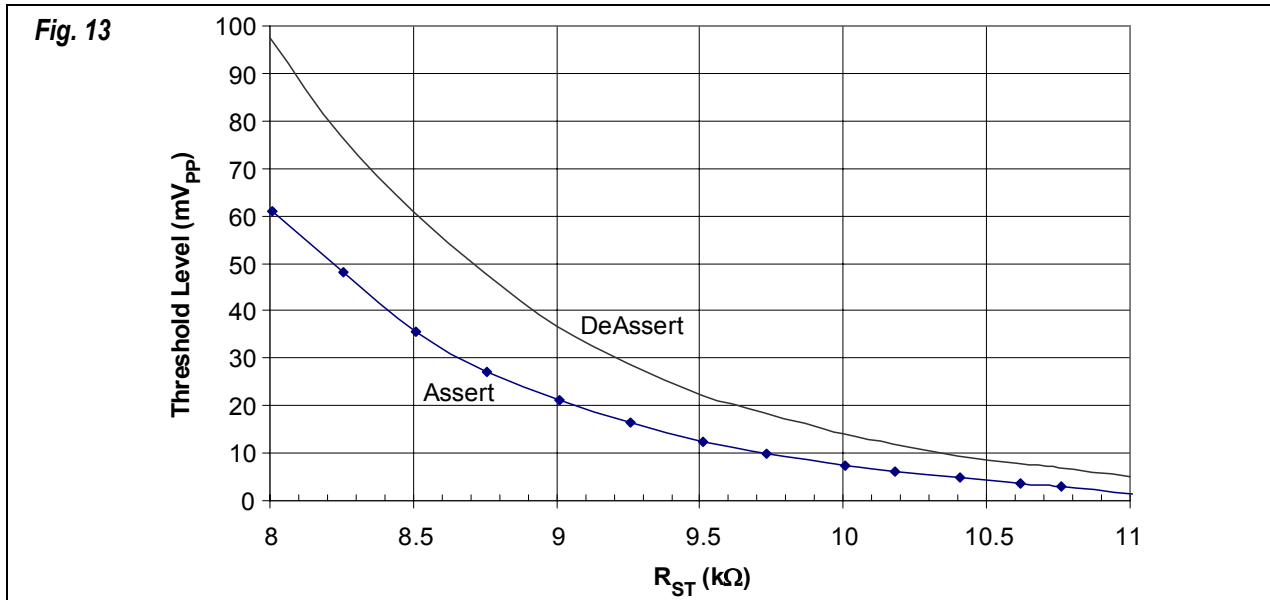
From Fig. 13, it is apparent that small variations in R_{LOS} cause significant variation in the LOS threshold level, particularly for low input signal levels. This is because of the logarithmic relationship between the RSSI voltage and the input signal level. It is recommended that a 1% resistor be used for R_{ST} and that allowance is provided for LOS variation, particularly when the LOS threshold is near the sensitivity limit of the M02040.

Example R_{ST} resistor values are given in Table 7.

TABLE 7 R_{ST} RESISTOR VALUES

VIN (mV pp) differential	R_{ST} (k Ω)
6.6	10.2
13	9.53
20	9.10
39	8.45
60	8.06

LOSS OF SIGNAL CHARACTERISTIC



3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

APPLICATIONS INFORMATION

PECLP and PECLN Termination

The outputs of the M02040 are PECL compatible and any standard AC or DC-coupling termination technique can be used. Fig. 14 and 15 illustrate typical AC and DC terminations.

AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drift and compatibility with non-PECL interfaces. Fig. 14 shows the circuit configuration and Table 8 lists the resistor values. If using transmission lines other than 50 Ω, the shunt terminating resistance Z_T

should equal twice the impedance of the transmission line (Z_0).

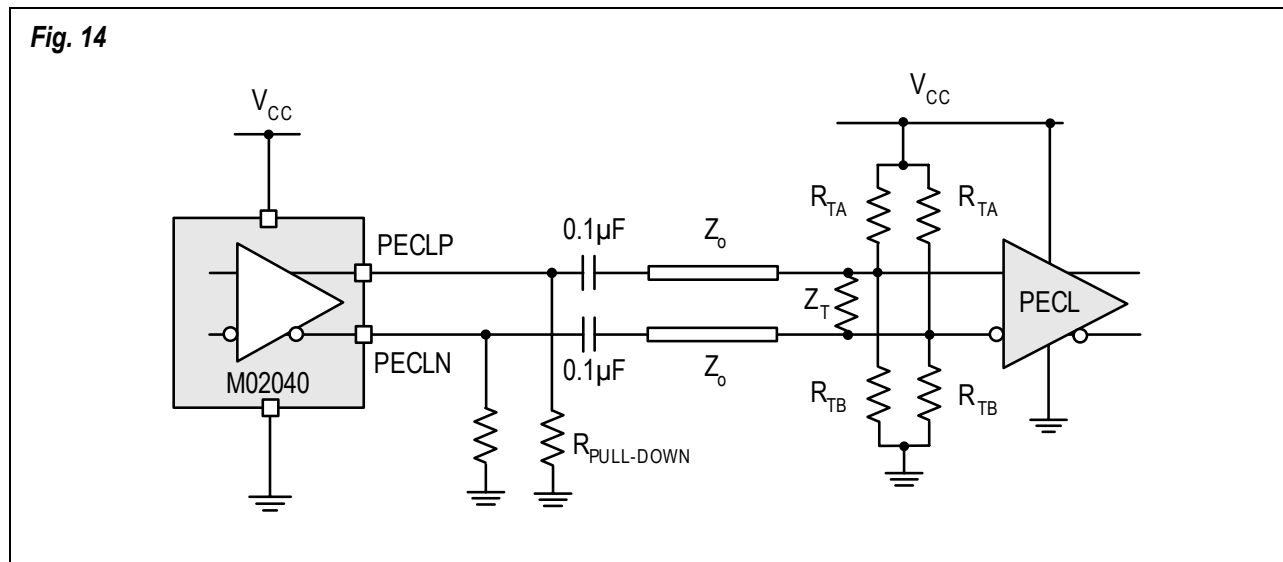
DC-coupling can be used when driving PECL interfaces and has the advantage of a reduced component count. A Thevenin termination is used at the receive end to give a 50 Ω load and the correct DC bias. Fig. 15 shows the circuit configuration and Table 8 the resistor values.

Alternatively, if available, terminating to $V_{CC} - 2V$ as shown in Fig. 16 has the advantage that the resistance value is the same for 3.3 V and 5 V operation and it also has performance advantages at high data rates.

TABLE 8 PECL TERMINATION RESISTOR VALUES

Supply	Output Impedance	$R_{PULL-DOWN}$	Z_T	R_{TA} / R_{TB}	R_T / R_B
5 V	50 Ω	270 Ω	100 Ω	2.7 kΩ / 7.8 kΩ	82 Ω / 130 Ω
3.3 V	50 Ω	150 Ω	100 Ω	2.7 kΩ / 4.3 kΩ	130 Ω / 82 Ω

AC-COUPLED PECL TERMINATION

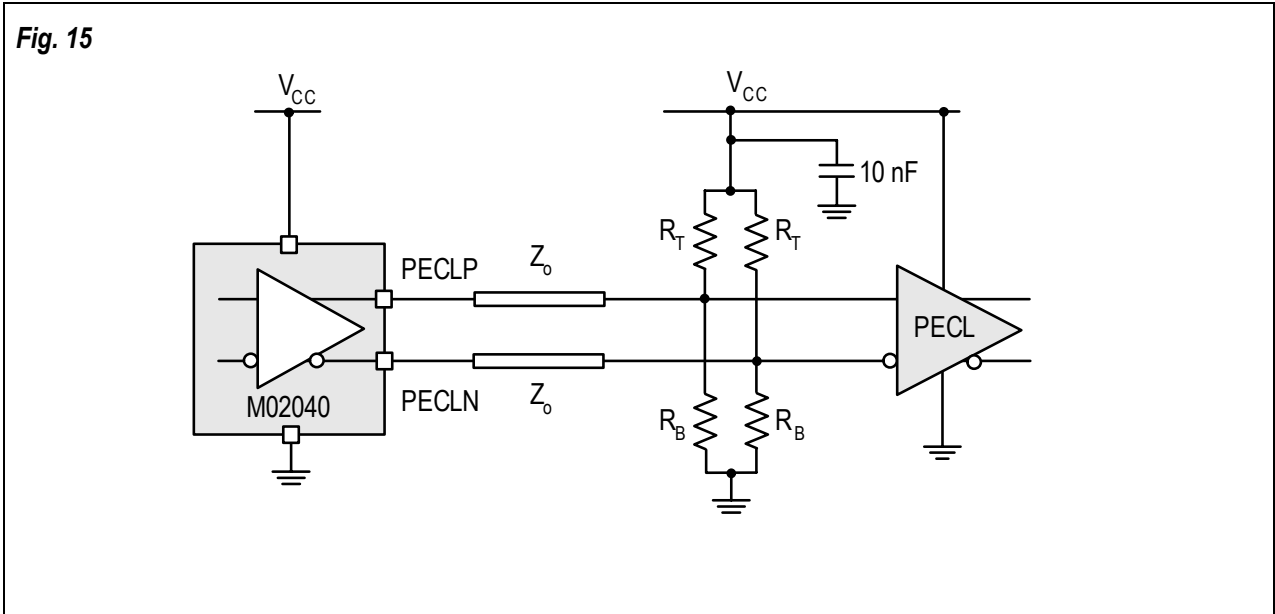


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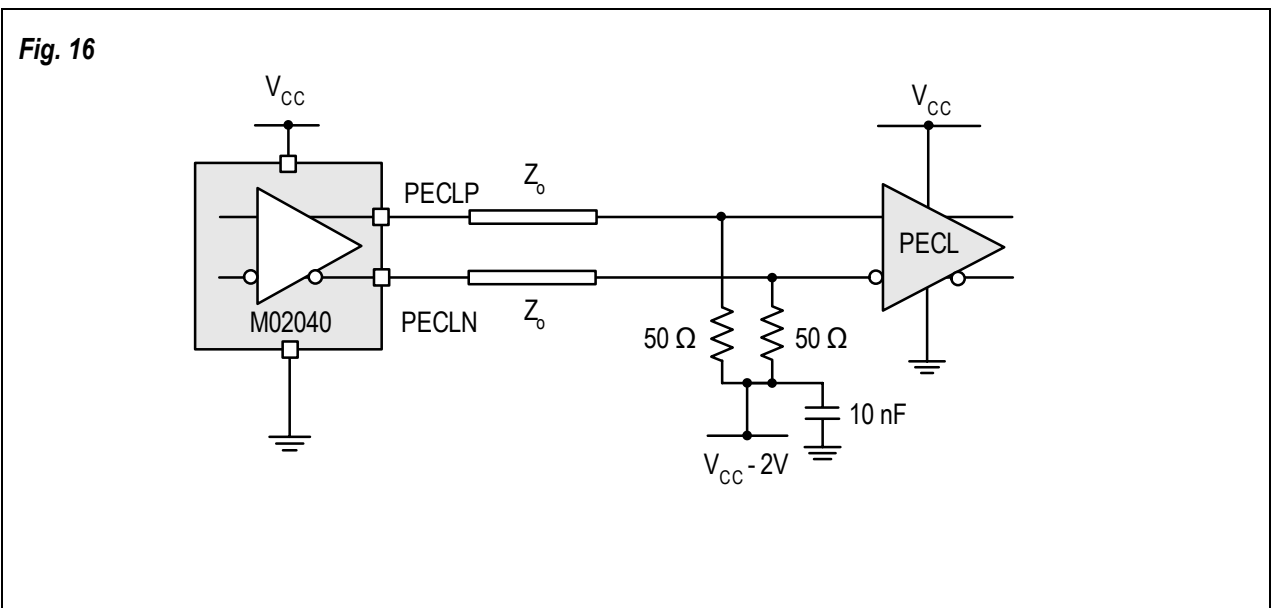
APPLICATIONS INFORMATION

DC-COUPLED PECL TERMINATION

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ALTERNATIVE PECL TERMINATION

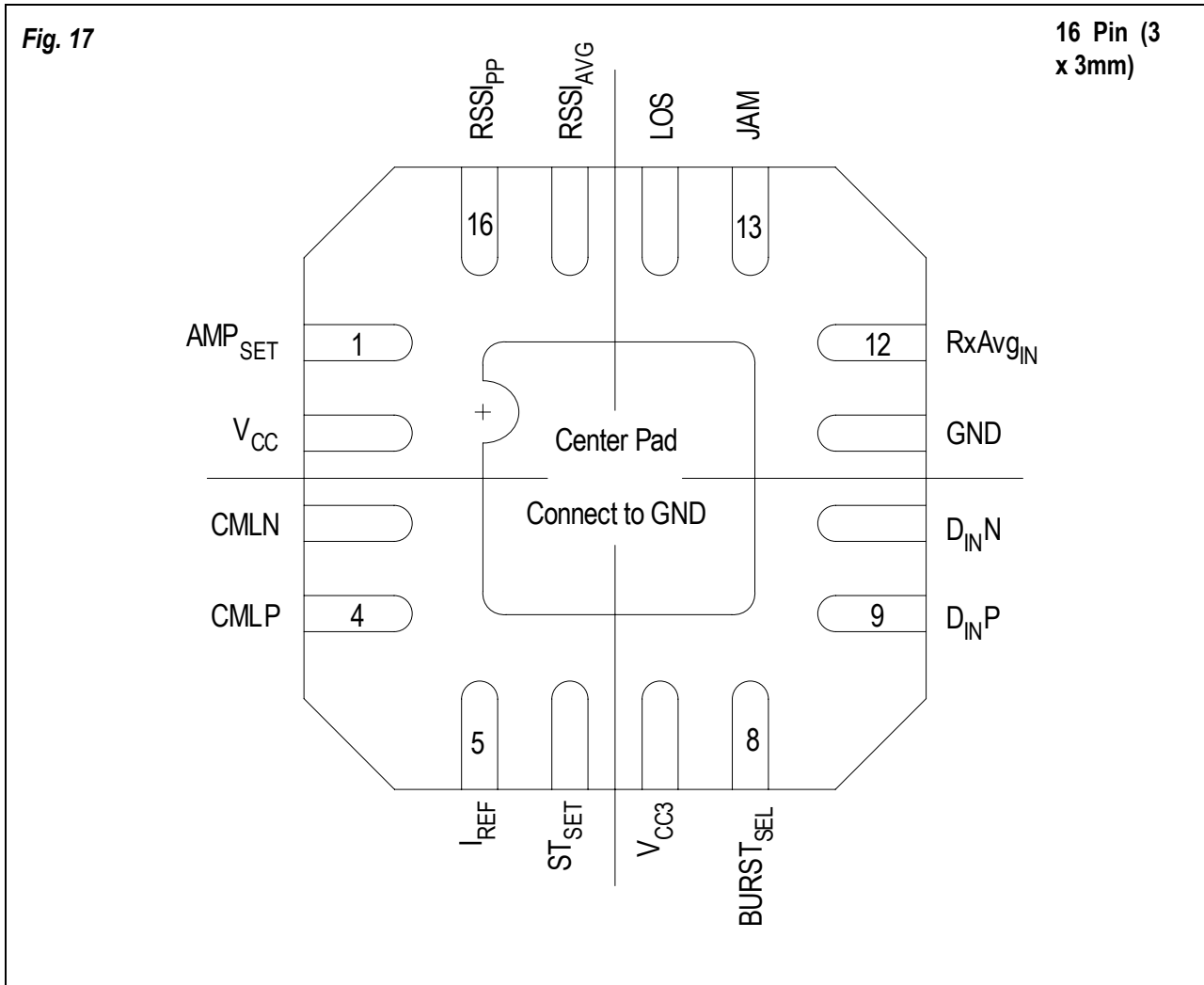


3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

PACKAGE PINOUT

M02040 PINOUT

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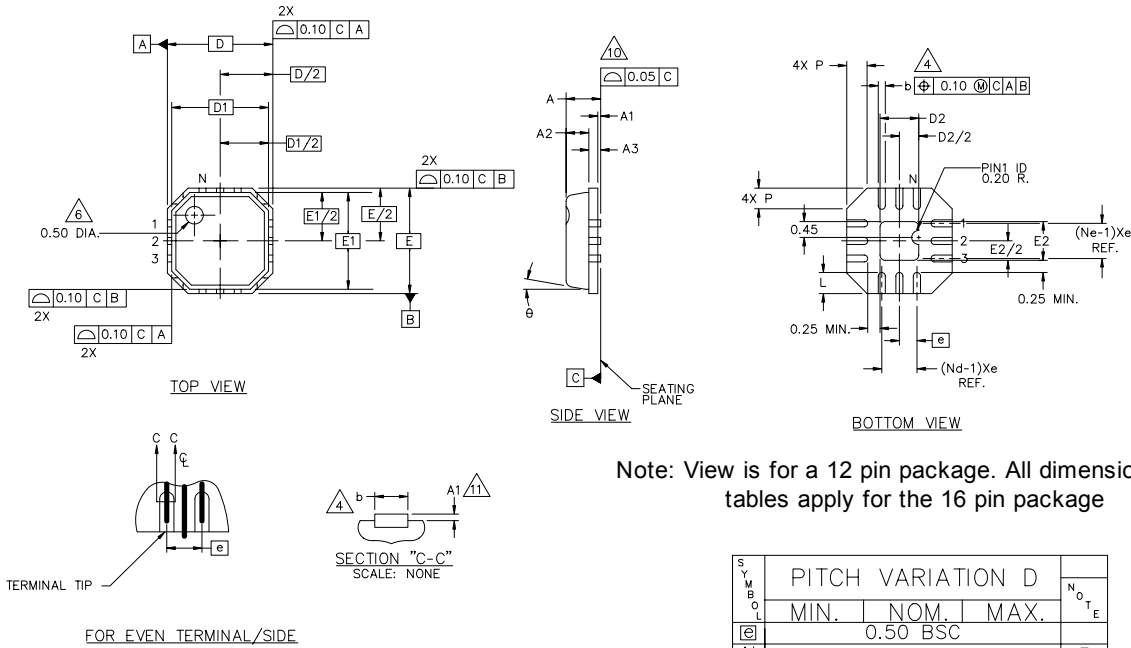


3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

PACKAGE INFORMATION

Advance Information

Fig. 18



Note: View is for a 12 pin package. All dimensions in the tables apply for the 16 pin package

SYMBOL	COMMON DIMENSIONS			N _{OTE}
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3		0.20 REF.		
D		3.00 BSC		
D1		2.75 BSC		
E		3.00 BSC		
E1		2.75 BSC		
θ			12°	
P	0.24	0.42	0.60	

SYMBOL	PITCH VARIATION D			N _{OTE}
	MIN.	NOM.	MAX.	
Ⓞ	0.50 BSC			
N	16			3
N _d	4			3
N _e	4			3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	1.35	1.50	1.65	
E2	1.35	1.50	1.65	

- NOTES:
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
 3. N IS THE NUMBER OF TERMINALS.
N_d IS THE NUMBER OF TERMINALS IN X-DIRECTION &
N_e IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
 4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
 6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
 7. ALL DIMENSIONS ARE IN MILLIMETERS.
 8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL 1/0.
 9. PACKAGE WARPAGE MAX 0.05mm.
 10. APPLIED FOR EXPOSED PAD AND TERMINALS.
EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
 11. APPLIED ONLY FOR TERMINALS.

3.3/5V Limiting Amplifier for Applications to 2.5 Gbps

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