

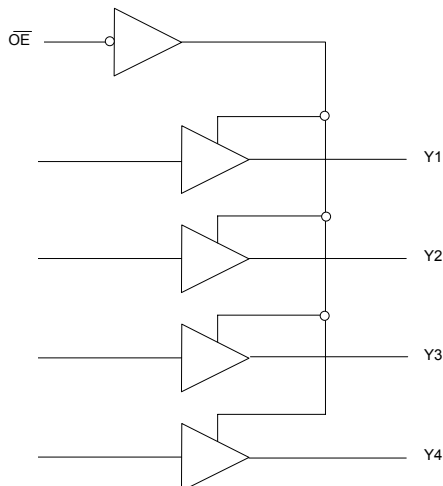


54LVTH162244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

Features

- Mixed-mode signal operation. (5V input/output with 3.3V supply).
- Total dose hardness: Typical 100 krad (Si), depending upon space environment
- Output ports have equivalent 22 ohm series resistors. External resistors not required.
- Unregulated battery operation down to 2.7V
- Typical V_{olp} (Output ground bounce) $< 0.8V$ at $V_{cc} = 3.3V$, $T_A = 25C$.
- Hot insertion supported.
- Bus hold on data inputs eliminates the need for external pullup/pulldown resistors.
- Distributed V_{cc} and GND pins minimize high speed switching noise.
- Flow-through architecture optimizes PCB layout
- Package:
48 pin flat pack shielded or unshielded package.

LOGIC DIAGRAM



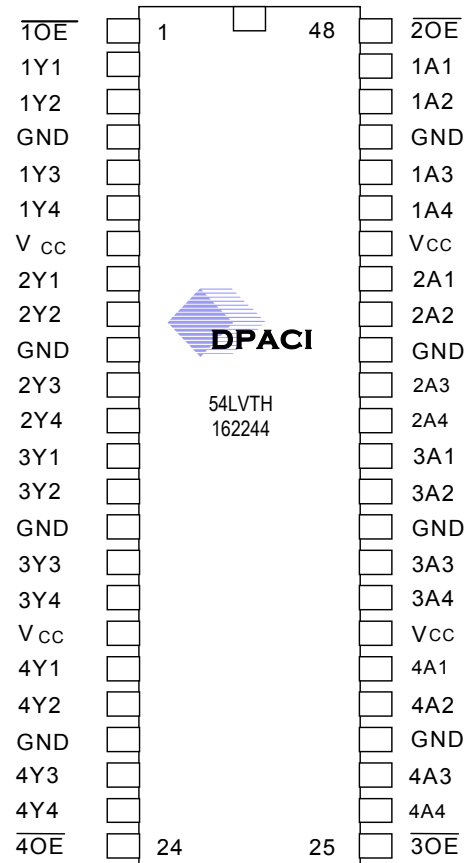
DPACI

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General Description

54LVTH162244 is a 16-bit buffer and line driver designed for low voltage operation with the capability to interface with a TTL environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs. The outputs which are designed to source or sink up to 12ma, include equivalent 22 ohm series resistors to reduce overshoot and undershoot. Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

DPACI incorporates radiation package shielding when required (based upon orbit requirements).



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ABSOLUTE MAXIMUM RATINGS ¹

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply voltage range	V_{CC}	-0.5	4.6	V
Input voltage range (see note 2)	V_I	-0.5	7.0	V
Voltage range applied to any output in the high impedance or power-off state (see note 2)	V_O	-0.5	7.0	V
Voltage range applied to any output in the high state (see note 2)	V_O	-0.5	$V_{CC} + .05$	V
Current into any output in the low state	I_O	--	30	mA
Current into any output in the high state(see note 3)	I_O	--	30	mA
Input clamp current	$I_{IK} (V_I < 0)$	--	-50	mA
Output clamp current	$I_{OK} (V_O < 0)$	--	-50	mA
Storage temperature range	T_S	-65	150	°C
Operating temperature range	T_A	-55	125	°C

RECOMMENDED OPERATING CONDITIONS⁴

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	2.7	3.6	V
High-level input voltage	V_{IH}	2	--	V
Low-level input voltage	V_{IL}	--	0.8	V
Input voltage	V_I	--	5.5	V
High-level output current	I_{OH}	--	-12	mA
Low level output current	I_{OL}	--	12	mA
Input transition rise or fall rate (outputs enabled)	$\Delta t/\Delta V$	--	10	ns/V
Power-up ramp rate	$\Delta t/\Delta V_{CC}$	200	--	us/V
Operating temperature	T_A	-55	125	°C

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This current flows only when the output is in the high state and $V_O > V_{CC}$.
4. All unused control inputs of the devices must be held at V_{CC} or GND to ensure proper device operation

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DC ELECTRICAL CHARACTERISTICS¹

(V_{CC}=3.3V ± 10%, T_a = -55 to +125 °C, C_L=50pF, unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V _{IK}		V _{CC} = 2.7V	I _I = -18mA	--	-1.2	V
V _{OH}		V _{CC} = 3V	I _{OH} = -12mA	2	--	V
V _{OL}		V _{CC} = 3V	I _{OL} = 12mA	--	0.8	V
I _I	CONTROL INPUTS	V _{CC} = 0 or 3.6V,	V _I = 5.5 V	--	10	μA
	DATA INPUTS	V _{CC} = 3.6V	V _I = V _{CC} or GND	--	±1	
			V _I = 0	--	-5	
I _{I(hold)}	DATA INPUTS	V _{CC} = 3 V	V _I = 0.8 V	75	--	μA
			V _I = 2 V	-75	--	
I _{OZH}		V _{CC} = 3.6 V	V _O = 3 V	--	5	μA
I _{OZL}		V _{CC} = 3.6 V	V _O = 0.5 V	--	-5	μA
I _{OZPU} ²		V _{CC} = 1.5V to 0, V _O = 0.5 V to 3 V, OE = don't care		--	±100	μA
I _{OZPD} ²		V _{CC} = 1.5V to 0, V _O = 0.5 V to 3 V, OE = don't care		--	±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	--	0.19	mA
			Outputs low	--	5	
			Outputs disabled	--	0.19	
ΔI _{CC} ¹		V _{CC} = 3 V to 3.6 V, One input at V _{CC} -0.6 V, Other inputs at V _{CC} or GND			0.2	mA
C _i ²		V _I = 3 V or 0		--	8	pF
C _o ²		V _O = 3 V or 0		--	15	pF

1 : This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND

2 : Guaranteed by Design

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = -55 to +125 °C, C_L = 50 pF, unless otherwise specified)

PARAMETER	SYMBOL	V _{CC} = 3.3 V		V _{CC} = 2.7 V	UNIT
		MIN	MAX	MAX	
Propogation Delay Time A to Y	t _{PLH}	1.1	4.6	5.1	ns
	t _{PHL}	1.1	3.9	4.5	
Output Enable Time OE to Y	t _{PZH}	1.1	5.4	6.7	ns
	t _{PZL}	1.3	4.9	6.1	
Output Disable Time OE to Y	t _{PHZ}	1.6	5.9	6.5	ns
	t _{PLZ}	1	5.9	5.8	

FUNCTION TABLE (each 4-bit buffer)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

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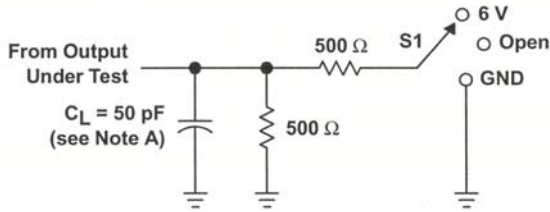
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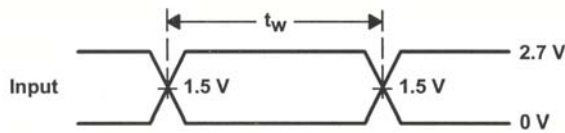


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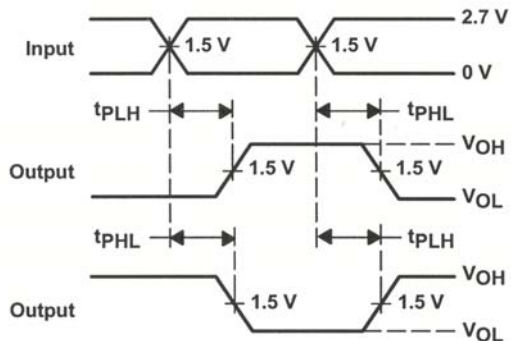
LOAD CIRCUIT AND VOLTAGE WAVEFORMS



LOAD CIRCUIT

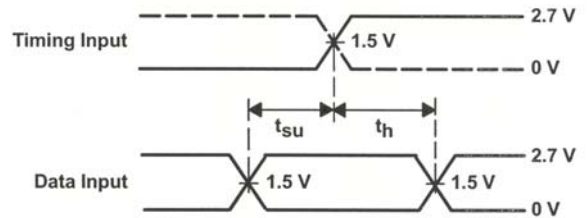


VOLTAGE WAVEFORMS
PULSE DURATION

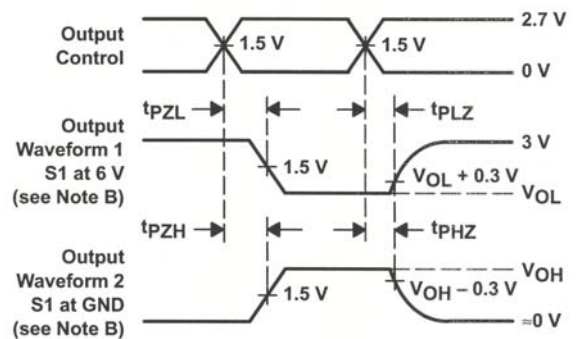


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

D. The outputs are measured one at a time with one transition per measurement.

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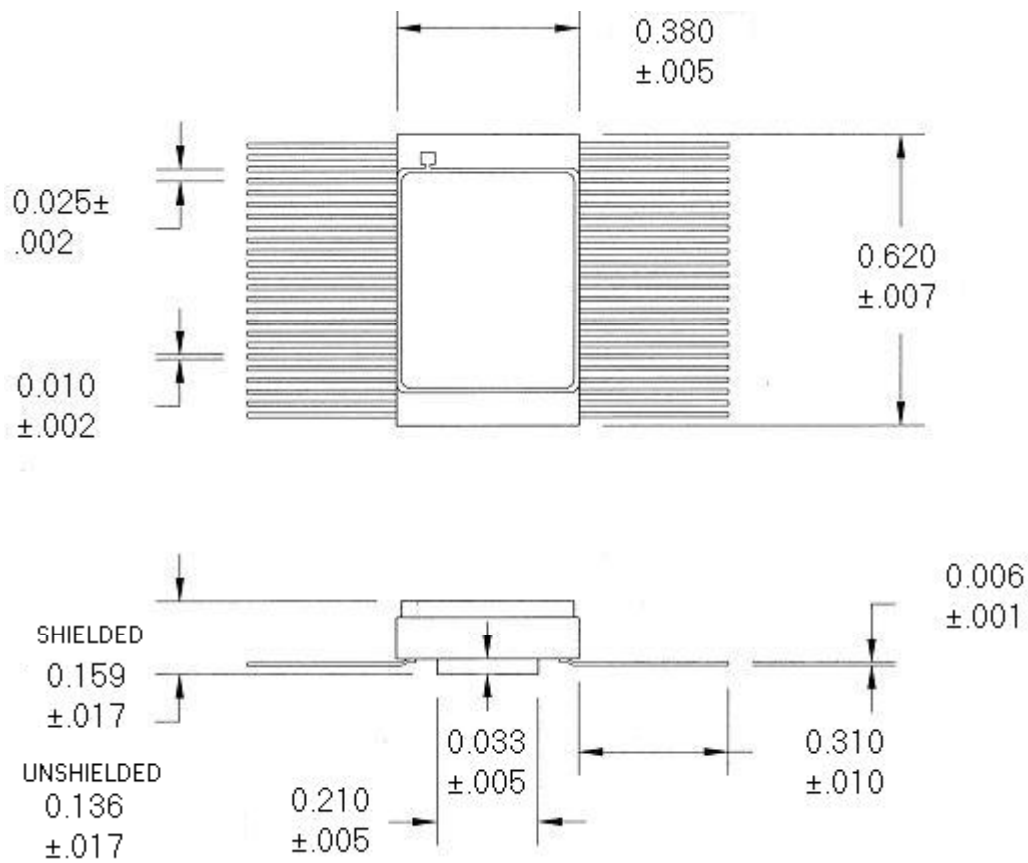
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48 PIN FLAT PACKAGE



NOTE: ALL DIMENSIONS ARE IN INCHES

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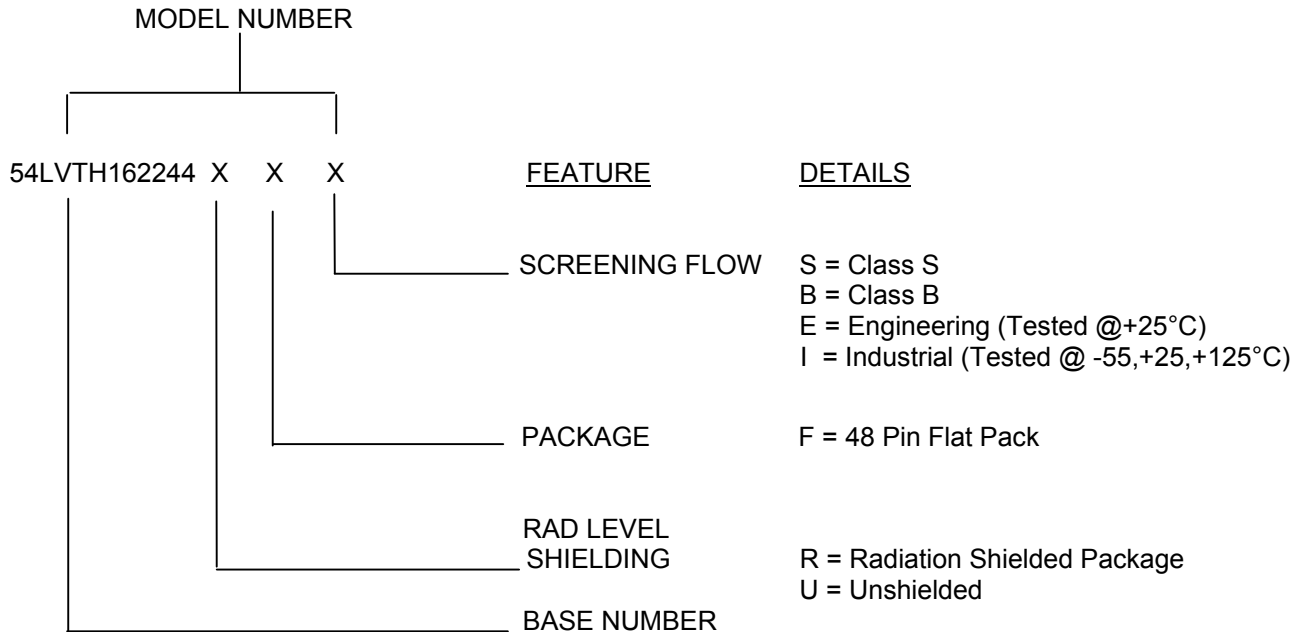
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PRODUCT ORDERING OPTIONS



Important notice:

These data sheets were created using the chip manufacturer’s published specifications. DPACI verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and DPACI assumes no responsibility for the use of this information.

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