

# FAST 74F899

## Dual Latch Transceiver with Parity

### FAST Products

### FEATURES

- Combines 'F543 and 'F280 functions into one package
- Combines 'F657 and 'F373 functions into one package (No need to change T/R to check parity)
- Output sink of 24 mA for the A-Bus and 64 mA for the B-bus
- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/EVEN parity
- Continuously checks parity of both A bus and B bus latches as  $\overline{ERRA}$  and  $\overline{ERRB}$
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data

### DESCRIPTION

The 'F899 is a 9-bit to 9-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the SEL input. Parity error checking of the

9-Bit Dual Latch Transceiver With 8-bit Parity  
Generator/Checker (3-State Outputs)  
*Preliminary Specification*

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F899	8.0ns	150mA

### ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
28-Pin Plastic DIP (600mil)	N74F899N
28-Pin PLCC	N74F899A

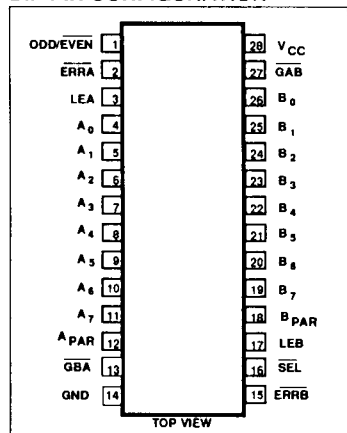
### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	Latched A bus 3-State inputs	3.5/0.117	70 $\mu$ A/70 $\mu$ A
$B_0 - B_7$	Latched B bus 3-State inputs	3.5/0.117	70 $\mu$ A/70 $\mu$ A
$A_{PAR}$	A bus parity 3-State input	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$B_{PAR}$	B bus parity 3-State input	1.0/0.033	20 $\mu$ A/20 $\mu$ A
ODD/EVEN	Parity Select Input (Low for EVEN parity)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$\overline{GBA}, \overline{GAB}$	Output Enable Inputs (Gate A to B, B to A)	2.0/0.066	40 $\mu$ A/40 $\mu$ A
SEL	Mode Select Input (Low for generate)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
LEA, LEB	Latch Enable Inputs (Low for latch)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$\overline{ERRA}, \overline{ERRB}$	Error Signal Outputs (active Low)	150/40	3mA/24mA
$A_0 - A_7$	A bus 3-State outputs	150/40	3mA/24mA
$B_0 - B_7$	B bus 3-State outputs	750/106.7	15mA/64mA
$A_{PAR}$	A bus parity 3-State output	150/40	3mA/24mA
$B_{PAR}$	B bus parity 3-State output	750/106.7	15mA/64mA

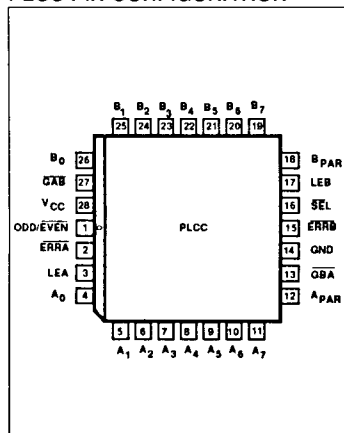
### NOTE:

One (1.0) FAST Unit Load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

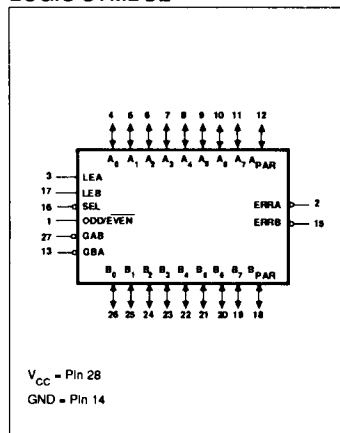
### DIP PIN CONFIGURATION



### PLCC PIN CONFIGURATION



### LOGIC SYMBOL



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A and B bus latches is continuously provided with  $\overline{ERRA}$  and  $\overline{ERRB}$ , even with both buses in 3-State. The device has a guaranteed current

sinking capability of 24 mA for the A-bus and 64 mA for the B-bus. Otherwise, the part is symmetrical (A and B bus functions are identical).

The 'F899 features independent latch enables for the A and B bus latches, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

**FUNCTIONAL DESCRIPTION:**

The 'F899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

**Transparent latch, Generate parity, Check A and B bus parity:**

Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as  $B_{PAR}$  ( $A_{PAR}$ ). If LEA

and LEB are High and the Mode Select ( $\overline{SEL}$ ) is Low, the parity generated from  $A_0$ - $A_7$  and  $B_0$ - $B_7$  can be checked and monitored by  $\overline{ERRA}$  and  $\overline{ERRB}$ . (Fault detection on both input and output buses.)

**Transparent latch, Feed-through parity, Check A and B bus parity:**

Bus A (B) communicates to Bus B (A) in a feed-through mode if  $\overline{SEL}$  is High. Parity is still generated and checked as  $\overline{ERRA}$  and  $\overline{ERRB}$  and can be used as

an interrupt to signal a data/parity bit error to the CPU.

**Latched input, Generate/Feed-through parity, Check A (and B) bus parity:**

Independent latch enables (LEA and LEB) allow other permutations of:

Transparent latch / 1bus latched / both busses latched  
Feed-through parity / generate parity  
Check in bus parity / check out bus parity / check in and out bus parity  
See function table below.

**FUNCTION TABLE**

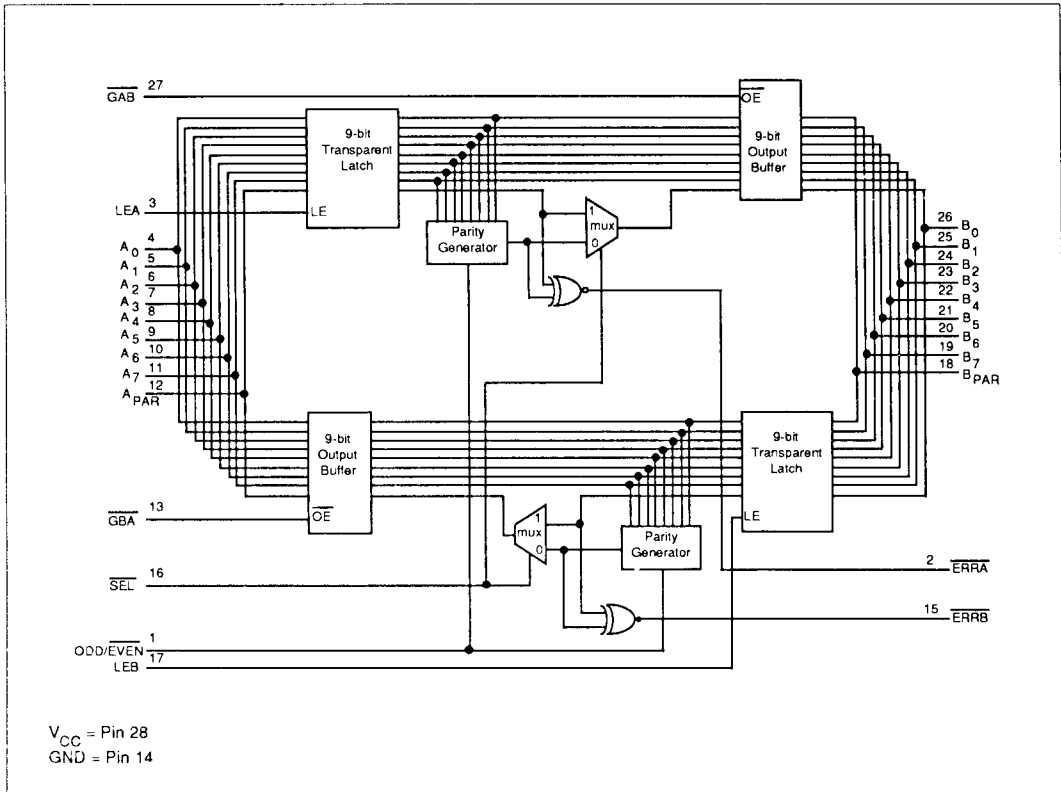
INPUTS					OPERATING MODE
GAB	GBA	SEL	LEA	LEB	
H	H	X	X	X	3-state A bus and B bus (Input A & B simultaneously)
H	L	L	L	H	B → A, Transparent B latch, Generate parity from $B_0$ - $B_7$ , Check B bus parity
H	L	L	H	H	B → A, Transparent A & B latch, Generate parity from $B_0$ - $B_7$ , Check A & B bus parity
H	L	L	X	L	B → A, B bus latched, Generate parity from latched $B_0$ - $B_7$ data, Check B bus parity
H	L	H	X	H	B → A, Transparent B latch, Parity feed-through, Check B bus parity
H	L	H	H	H	B → A, Transparent A & B latch, Parity feed-through, Check A & B bus parity
L	H	L	H	X	A → B, Transparent A latch, Generate parity from $A_0$ - $A_7$ , Check A bus parity
L	H	L	H	H	A → B, Transparent A & B latch, Generate parity from $A_0$ - $A_7$ , Check A & B bus parity
L	H	L	L	X	A → B, A bus latched, Generate parity from latched $A_0$ - $A_7$ data, Check A bus parity
L	H	H	H	L	A → B, Transparent A latch, Parity feed-through, Check A bus parity
L	H	H	H	H	A → B, Transparent A & B latch, Parity feed-through, Check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level  
L = Low voltage level  
X = Don't care

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## BLOCK DIAGRAM



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**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to + $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	$A_0 - A_7, A_{PAR}, \overline{ERRA}, \overline{ERRB}$	48
		$B_0 - B_7, B_{PAR}$	128
$T_A$	Operating free-air temperature range	0 to +70	°C
$T_{STG}$	Storage temperature	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current	$A_0 - A_7$		-3	mA
		$B_0 - B_7$		-15	
$I_{OL}$	Low-level output current	$A_0 - A_7$		24	mA
		$B_0 - B_7$		64	
$T_A$	Operating free-air temperature range	0		70	°C

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**DC ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>			LIMITS			UNIT
						Min	Typ <sup>2</sup>	Max	
$V_{OH}$	High-level output voltage	All outputs	$V_{CC} = \text{MIN.}$ $V_{IL} = \text{MAX.}$ $V_{IH} = \text{MIN.}$	$I_{OH} = -3\text{mA}$	$\pm 10\%V_{CC}$	2.4			V
					$\pm 5\%V_{CC}$	2.7	3.4		V
		$B_0$ - $B_7$ , $B_{PAR}$	$V_{CC} = \text{MIN.}$ $V_{IL} = \text{MAX.}$ $V_{IH} = \text{MIN.}$	$I_{OH} = -15\text{mA}$	$\pm 10\%V_{CC}$	2.0			V
					$\pm 5\%V_{CC}$	2.0			V
$V_{OL}$	Low-level output voltage	$A_0$ - $A_7$ , $A_{PAR}$ , $\overline{ERRA}$ , $\overline{ERRB}$	$V_{CC} = \text{MIN.}$ $V_{IL} = \text{MAX.}$ $V_{IH} = \text{MIN.}$	$I_{OL} = 24\text{mA}$	$\pm 10\%V_{CC}$		0.35	0.50	V
					$\pm 5\%V_{CC}$		0.35	0.50	V
		$B_0$ - $B_7$ , $B_{PAR}$	$V_{CC} = \text{MIN.}$ $V_{IL} = \text{MAX.}$ $V_{IH} = \text{MIN.}$	$I_{OL} = 48\text{mA}$	$\pm 10\%V_{CC}$		0.38	0.55	V
					$\pm 5\%V_{CC}$		0.42	0.55	V
$V_{IK}$	Input clamp voltage		$V_{CC} = \text{MIN.}, I_1 = I_{IK}$			-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage	Other Inputs	$V_{CC} = 0.0\text{V}, V_I = 7.0\text{V}$				100	$\mu\text{A}$	
		$A_0$ - $A_7$ , $A_{PAR}$	$V_{CC} = \text{MAX.}, V_I = 5.5\text{V}$				2.0	mA	
		$B_0$ - $B_7$ , $B_{PAR}$					1.0	mA	
$I_{IH}$	High-level input current	$\text{ODD/EVEN, SEL, LEA, LEB}$	$V_{CC} = \text{MAX.}, V_I = 2.7\text{V}$				20	$\mu\text{A}$	
		$\overline{\text{GAB}}, \overline{\text{GBA}}$					40	$\mu\text{A}$	
$I_{IL}$	Low-level input current	$\text{ODD/EVEN, SEL, LEA, LEB}$	$V_{CC} = \text{MAX.}, V_I = 0.5\text{V}$				-20	$\mu\text{A}$	
		$\overline{\text{GAB}}, \overline{\text{GBA}}$					-40	$\mu\text{A}$	
$I_{IH} + I_{OZH}$	Off-state output current High-level voltage applied	$A_0$ - $A_7$ , $A_{PAR}$	$V_{CC} = \text{MAX.}, V_O = 2.7\text{V}$				70	$\mu\text{A}$	
$I_{IL} + I_{OZL}$	Off-state output current Low-level voltage applied	$B_0$ - $B_7$ , $B_{PAR}$	$V_{CC} = \text{MAX.}, V_O = 0.5\text{V}$				-70	$\mu\text{A}$	
$I_{OZH}$	Off-state output current High-level voltage applied	$\text{ODD/EVEN, SEL, LEA, LEB}$	$V_{CC} = \text{MAX.}, V_{IH} = \text{MIN.}, V_O = 2.7\text{V}$				50	$\mu\text{A}$	
$I_{OZL}$	Off-state output current Low-level voltage applied	$\overline{\text{GAB}}, \overline{\text{GBA}}$	$V_{CC} = \text{MAX.}, V_{IH} = \text{MIN.}, V_O = 0.5\text{V}$				-50	$\mu\text{A}$	
$I_{OS}$	Short-circuit output current <sup>3</sup>	$A_0$ - $A_7$ , $A_{PAR}$	$V_{CC} = \text{MAX.}$				-60	-150	mA
		$B_0$ - $B_7$ , $B_{PAR}$					-100	-225	mA
$I_{CC}$	Supply current (total)	$I_{CCH}$	$V_{CC} = \text{MAX.}$				90	125	mA
		$I_{CCL}$					106	150	mA
		$I_{CCZ}$					98	145	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation delay (Transparent latch) $A_n$ to $B_n$ or $B_n$ to $A_n$	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay (Feed-through Parity) $A_{PAR}$ to $B_{PAR}$ or $B_{PAR}$ to $A_{PAR}$	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay (Generate Parity) $A_n, A_{PAR}$ to $B_{PAR}$ or $B_n, B_{PAR}$ to $A_{PAR}$	Waveform 1		10.0 10.0		8.0 8.0	15.0 15.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay (Check Parity) $A_n, A_{PAR}$ to $\overline{ERRA}$ or $B_n, B_{PAR}$ to $\overline{ERRB}$	Waveform 1		10.0 10.0		8.0 8.0	15.0 15.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay ODD/EVEN to $\overline{ERRA}$ , $\overline{ERRB}$ , $A_{PAR}$ , or $B_{PAR}$	Waveform 1		10.0 10.0		8.0 8.0	15.0 15.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay SEL to $A_{PAR}$ , $B_{PAR}$	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay LEA to $B_n, B_{PAR}$ or LEB to $A_n, A_{PAR}$	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
$t_{PZH}$ $t_{PZL}$	Output Enable time $\overline{GBA}$ to $A_n, A_{PAR}$ or $\overline{GAB}$ to $B_n, B_{PAR}$	Waveform 3, 4		10.0 10.0		8.0 8.0	15.0 15.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable time $\overline{GBA}$ to $A_n, A_{PAR}$ or $\overline{GAB}$ to $B_n, B_{PAR}$	Waveform 3, 4		10.0 10.0		8.0 8.0	15.0 15.0	ns

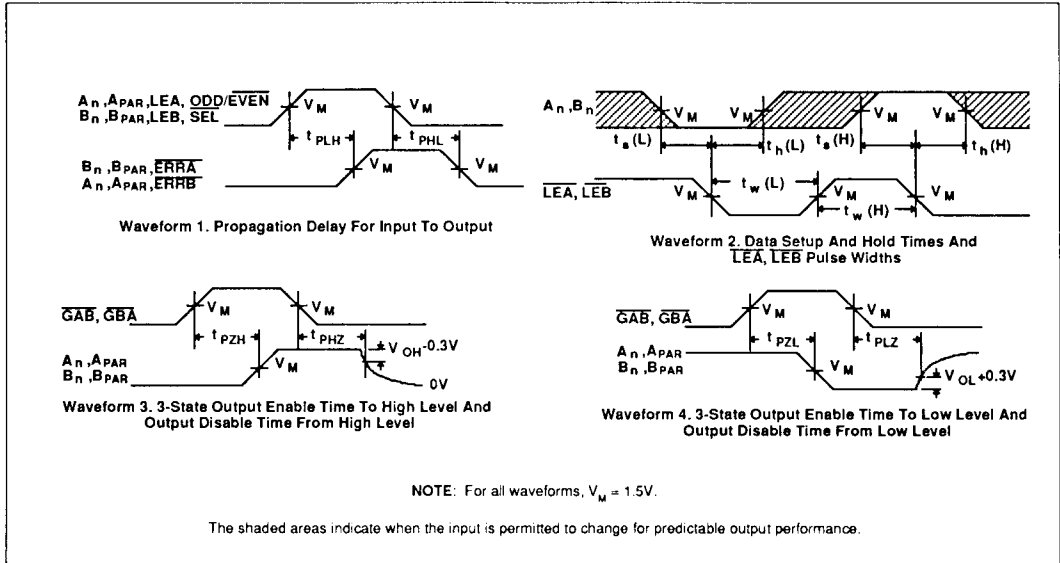
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time $A_n$ to LEA or $B_n$ to LEB	Waveform 2	3.0 3.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time $A_n$ to LEA or $B_n$ to LEB	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width LEA or LEB	Waveform 2	5.0 5.0			5.0 5.0		ns

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## AC WAVEFORMS



## TEST CIRCUIT AND WAVEFORMS

