The Analog Mixed Signal Company

Brief Data Sheet

Rev.1.41/ April 2013

ZSPM1000

True Digital PWM Controller (Single-Phase, Single-Rail)

Smart Power Management ICs

Power and Precision

ZSPM1000

True Digital PWM Controller (Single-Phase, Single-Rail)

The Analog Mixed Signal Company

Brief Description

The ZSPM1000 is a configurable true-digital single-phase PWM controller for high-current, non-isolated DC/DC supplies. It operates as a synchronous step-down converter in a single-rail and single-phase configuration.

The ZSPM1000 integrates a digital control loop, optimized for maximum flexibility and stability, as well as load step and steady-state performance. In addition, a rich set of protection and monitoring functions is provided. On-chip, non-volatile memory (NVM) and an I²C™ * interface facilitate configuration.

The PC-based ZMDI's Pink Power Designer™ provides a user-friendly and easy-to-use interface to the device for communication and configuration. It can guide the user through the design of the digital compensator and offers intuitive configuration methods for additional features, such as protection and sequencing.

Features

- Programmable digital control loop
- Advanced digital control techniques
  - Tru-sample Technology™
  - State-Law Control™ (SLC)
  - Sub-cycle Response™ (SCR)
- Improved transient response and noise immunity
- Protection features
  - Over-current protection
  - Over-voltage protection (VIN, VOUT)
  - Under-voltage protection (VIN, VOUT)
  - Overloaded startup
  - Restart and delay
- Support for SMOD and ZCD drivers
- Fuse-based NVM for improved reliability
- Operation from a single 5V or 3.3V supply
- Optional PMBus™ address selection without external resistors

Benefits

- Fast configurability and design flexibility
- Simplified design and integration
- Reduced component count through system level integration
- Simplified monitoring for system power and thermal management
- Higher energy efficiency across all output loading conditions

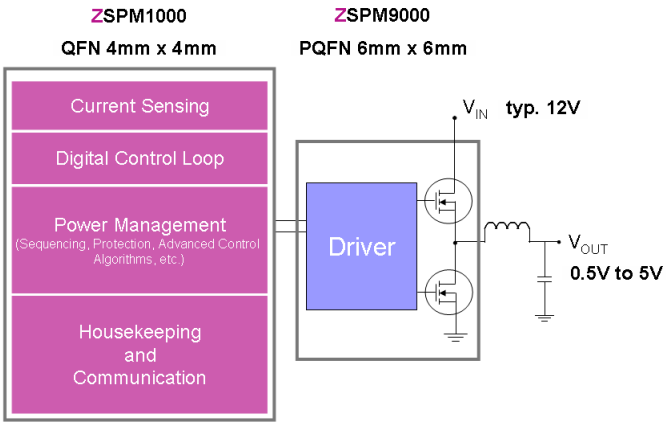
Available Support

- Evaluation Kit
- PC-based Pink Power Designer™

Physical Characteristics

- Operation temperature: -40°C to +125°C**
- V_{OUT} max: 5V
- Lead free (RoHS compliant) 24-pin QFN package (4 mm x 4 mm)

ZSPM1000 Typical Application Diagram



* I²C™ is a registered trademark of NXP.

** Subject to product type.

For more information, contact ZMDI via SPM@zmdi.com.

ZSPM1000

True Digital PWM Controller (Single-Phase, Single-Rail)

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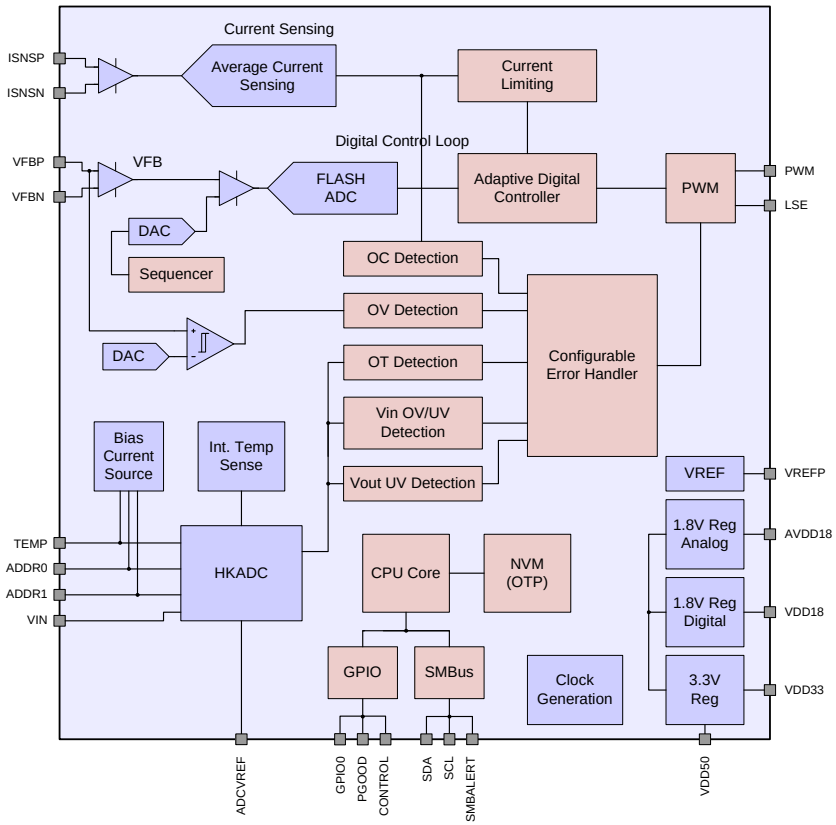
ZSPM1000 Block Diagram



Typical Applications

- *Telecom Switches*
- *Servers and Storage*
- *Base Stations*
- *Network Routers*
- *Industrial Applications*
- *Single-Rail/Single-Phase Supplies for Processors, ASICs, FPGAs, DSPs*

Ordering Information *(See additional options in section 7 of the ZSPM1000 Data Sheet.)*

Sales Code	Description	Package
ZSPM1000ZI1R 1	ZSPM1000 Lead-free QFN24 — Temperature range: -40°C to +85°C	Reel
ZSPM1000ZA1R 1	ZSPM1000 Lead-free QFN24 — Temperature range: -40°C to +125°C	Reel
ZSPM8000-KIT	Evaluation Kit for ZSPM1000 with PMBus™ Communication Interface and Pink Power Designer™ GUI	Kit

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1 IC Characteristics

1.1. Absolute Maximum Ratings

PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage	VDD50	dV/dt < 0.15V/µs	-0.3		5.5	V
Maximum slew rate					0.15	V/µs
3.3 V supply voltage	VDD33		-0.3		3.6	V
1.8 V supply voltage	VDD18 AVDD18		-0.3		2.0	V
Digital pins						
Digital I/O pins	SCL SCA SMBALERT GPIO0 CONTROL PGOOD LSE PWM		-0.3		5.5	V
Analog pins						
Current sensing	ISNSP, ISNSN		-0.3		5.5	V
Voltage feedback	VFBP VFBN		-0.3		2.0	V
All other analog pins	ADCVREF VREFP TEMP VIN ADDR0 ADDR1		-0.3		2.0	V
Ambient conditions						
Storage temperature	T_{STOR}		-40		150	°C

1.2. Recommended Operating Conditions

PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient conditions (depending on product type)						
Operation temperature	T_{AMB}		-40		125	°C
Operation temperature	T_{AMB}		-40		85	°C

1.3. Electrical Parameters

PARAMETER	PIN	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage	VDD50		4.75	5.0	5.25	V
5 V supply current		VDD50=5.0 V		23		mA
3.3 V supply voltage	VDD33		3.0	3.3	3.6	V
3.3 V supply current		VDD50=VDD33=3.3 V		23		mA
Internally generated supply voltages						
3.3 V supply voltage	VDD33	VDD50=5.0 V	3.0	3.3	3.6	V
3.3 V output current		VDD50=5.0 V			2.0	mA
1.8 V supply voltages	AVDD18 VDD18	VDD50=5.0 V	1.72	1.80	1.98	V
1.8 V output current					0	mA
Power on reset threshold – on	VDD33			2.8		V
Power on reset threshold – off				2.6		V
Digital IO pins (GPIO0, CONTROL, PGOOD)						
Input high voltage		VDD33=3.3 V	2.0			V
Input low voltage		VDD33=3.3 V			0.8	V
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Input leakage current					±1.0	µA
Output current – high					2.0	mA
Output current – low					2.0	mA
Digital IO pins with tri-state capability (LSE, PWM)						
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Output current – high					2.0	mA
Output current – low					2.0	mA
Tri-state leakage current					±1.0	µA
SMBus pins (SCL, SDA, SMBALERT) – open drain						
Input high voltage		VDD33=3.3 V	2.0			V
Input low voltage		VDD33=3.3 V			0.8	V
Maximum bus voltage					5.25	V
Output current – low					2.0	mA

PARAMETER	PIN	CONDITIONS	MIN	TYP	MAX	UNITS
Output voltage*						
Set-point voltage			0		1.4	V
Set-point resolution				1.4		mV
Set-point accuracy		VOUT=1.4 V		1		%
*Without external prescaler.						
Inductor current measurement						
Common mode voltage	ISNSP ISNSN		0		5.0	V
Differential voltage range	ISNSP - ISNSN				±100	mV
Accuracy				5		%
Recommended DCR sense voltage for maximum output current			10			mV
Digital pulse width modulator						
Switching frequency			177		1000	kHz
Resolution				163		ps
Frequency accuracy				2.0		%
Over-voltage protection						
Reference DAC						
Set-point voltage			0		1.58	V
Resolution				25		mV
Set point accuracy				2		%
Comparator						
Hysteresis				35		mV
HKADC input pins						
Input voltage	TEMP VIN ADDR0 ADDR1		0		1.44	V
Source impedance Vin sensing					3	kΩ
ADC resolution				0.7		mV

PARAMETER	PIN	CONDITIONS	MIN	TYP	MAX	UNITS
External temperature measurement						
Supported sense elements	PN-junction					
Bias currents for external temperature sensing	TEMP			60		µA
Resolution	TEMP			0.32		K
Accuracy of measurement	TEMP			±5.0		K
Internal temperature measurement						
Resolution				0.22		K
Accuracy of measurement				±5.0		K

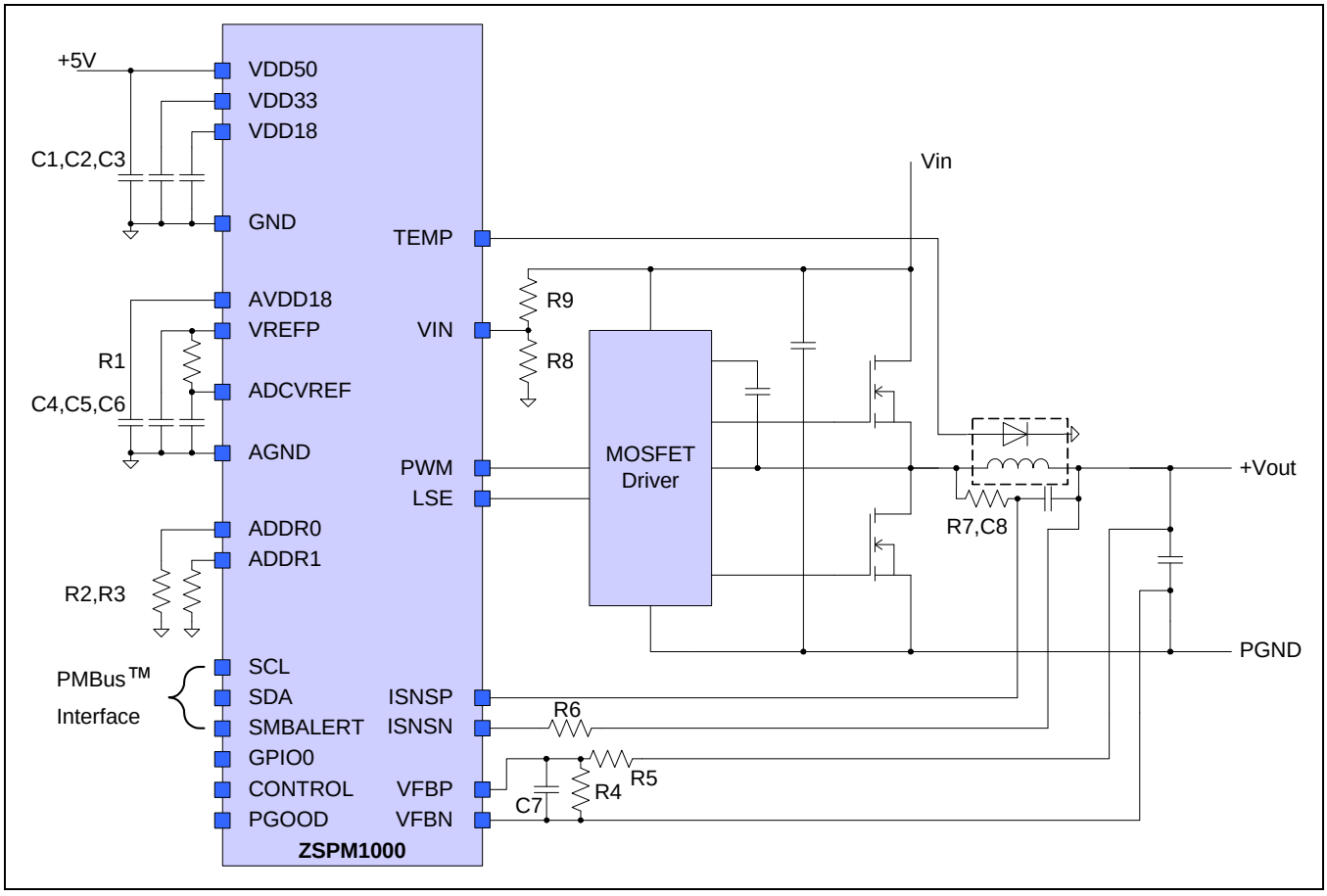
2 Product Summary

2.1. Overview

The ZSPM1000 is a configurable true-digital single-phase PWM controller for high-current, non-isolated DC/DC supplies supporting switching frequencies up to 1MHz. It offers a PMBus™ configurable digital power control loop incorporating output voltage sensing and average inductor current sensing, bundled with extensive fault monitoring and handling options.

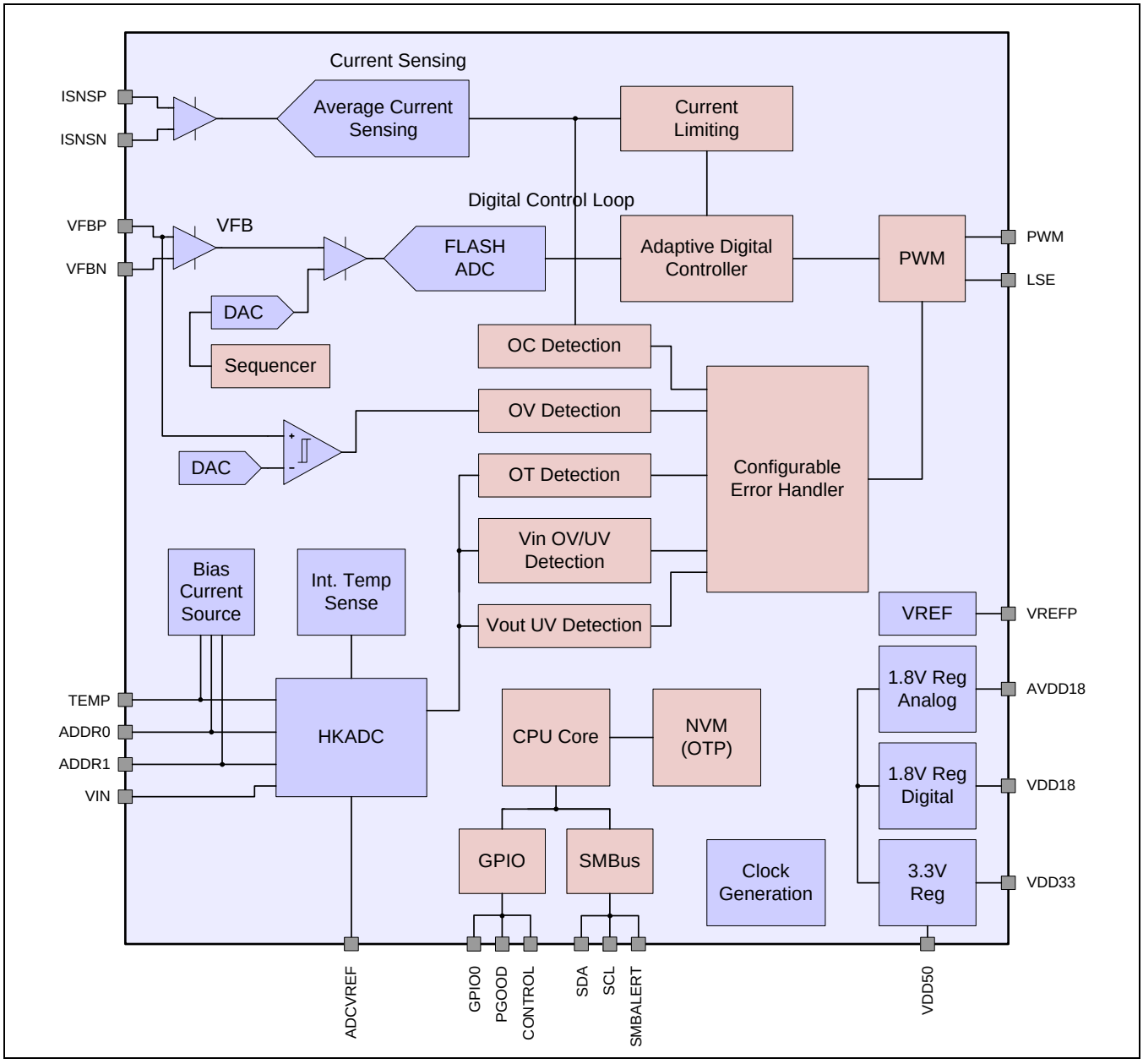
Several different functional units are incorporated in the device. A dedicated digital control loop is used to provide fast loop response and optimal output voltage regulation. This includes output voltage sensing, average inductor current sensing, a digital control law, and a digital pulse-width modulator (DPWM). In parallel, a dedicated, configurable error handler allows fast and flexible detection of error signals and their appropriate handling. A housekeeping analog-to-digital converter (HKADC) ensures the reliable and efficient measurement of environmental signals such as input voltage and temperature. An application-specific, low-energy microcontroller is used to control the overall system. Among other things, it manages configuration of the various logic units and handles the PMBus™ communication protocol. A PMBus™/SMBus/I²C™ interface is incorporated to connect with the outside world, supported by control and power-good signals.

Figure 2.1 Typical Application Circuit with a 5 V Supply Voltage



A high-reliability, high-temperature one-time programmable memory (OTP) is used to store configuration parameters. All required bias and reference voltages are internally derived from the external supply voltage.

Figure 2.2 Block Diagram

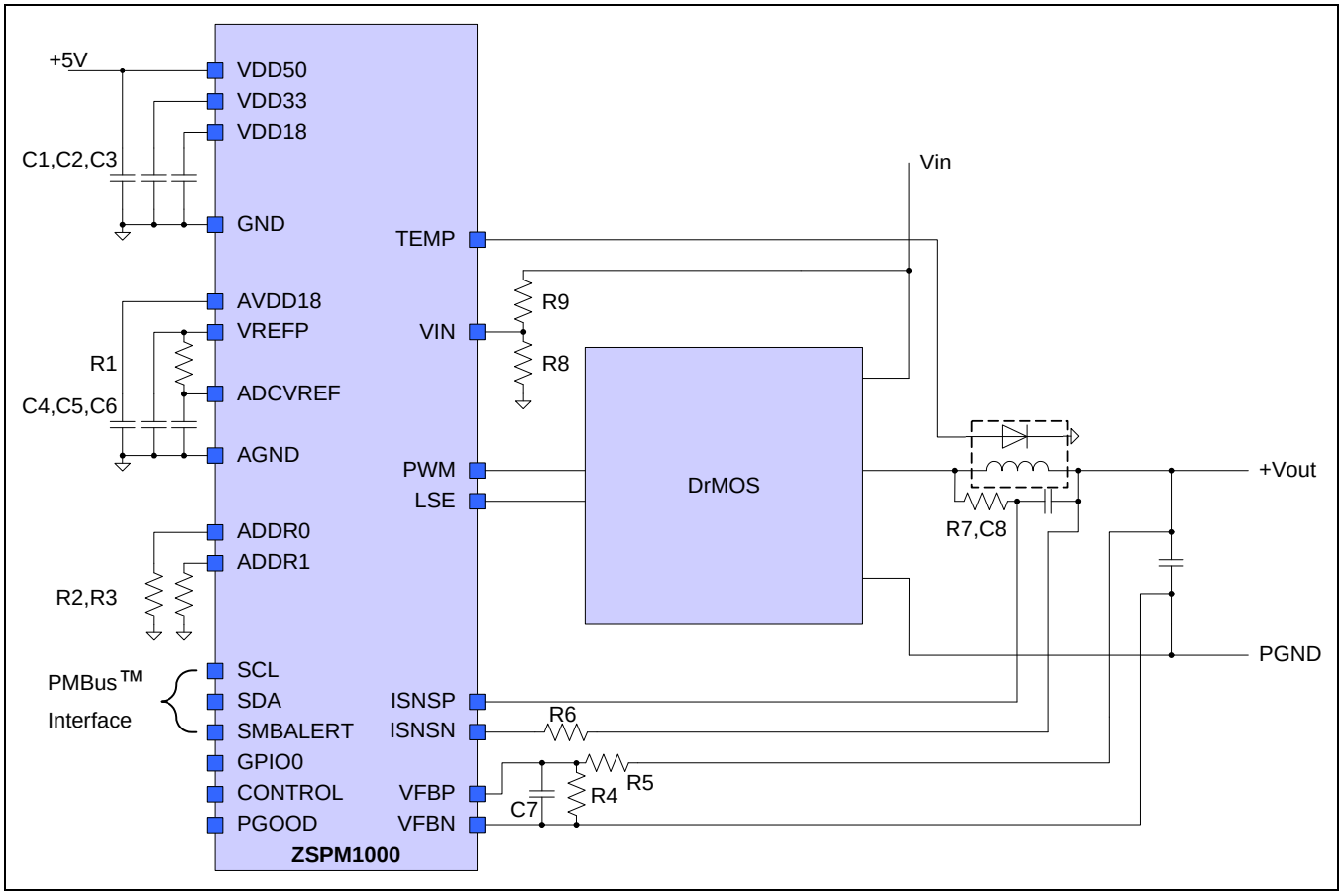


2.2. Pin Description

Pin	Name	Direction	Type	Description
1	AGND	Input	Supply	Analog Ground
2	VREFP	Output	Supply	Reference Terminal
3	VFBP	Input	Analog	Positive Input of Differential Feedback Voltage Sensing
4	VFBN	Input	Analog	Negative Input of Differential Feedback Voltage Sensing
5	ISNSP	Input	Analog	Positive Input of Differential Current Sensing
6	ISNSN	Input	Analog	Negative Input of Differential Current Sensing
7	TEMP	Input	Analog	Connection to External Temperature Sensing Element
8	VIN	Input	Analog	Power Supply Input Voltage Sensing
9	ADDR0	Input	Analog	SMBus Address Selection 0
10	ADDR1	Input	Analog	SMBus Address Selection 1
11	PWM	Output	Digital	High-side FET Control Signal
12	LSE	Output	Digital	Low-side FET Control Signal
13	PGOOD	Output	Digital	PGOOD Output (Internal Pull-Down)
14	CONTROL	Input	Digital	Control Input
15	GPIO0	Input/Output	Digital	General Purpose Input/Output Pin
16	SMBALERT	Output	PMBus™	SMBus Alert Output
17	SDA	Input/Output	PMBus™	SMBus Shift Data I/O
18	SCL	Input	PMBus™	SMBus Shift Clock Input (Slave-only)
19	GND	Input	Supply	Digital Ground
20	VDD18	Output	Supply	Internal 1.8 V Digital Supply Terminal
21	VDD33	Input/Output	Supply	3.3 V Supply Voltage Terminal
22	VDD50	Input	Supply	5.0 V Supply Voltage Terminal
23	AVDD18	Output	Supply	Internal 1.8 V Analog Supply Terminal
24	ADCVREF	Input	Analog	Analog-to-Digital Converter (ADC) Reference Terminal
PAD	PAD	Input	Supply	Exposed PAD, Digital Ground

2.3. Typical Application Circuit

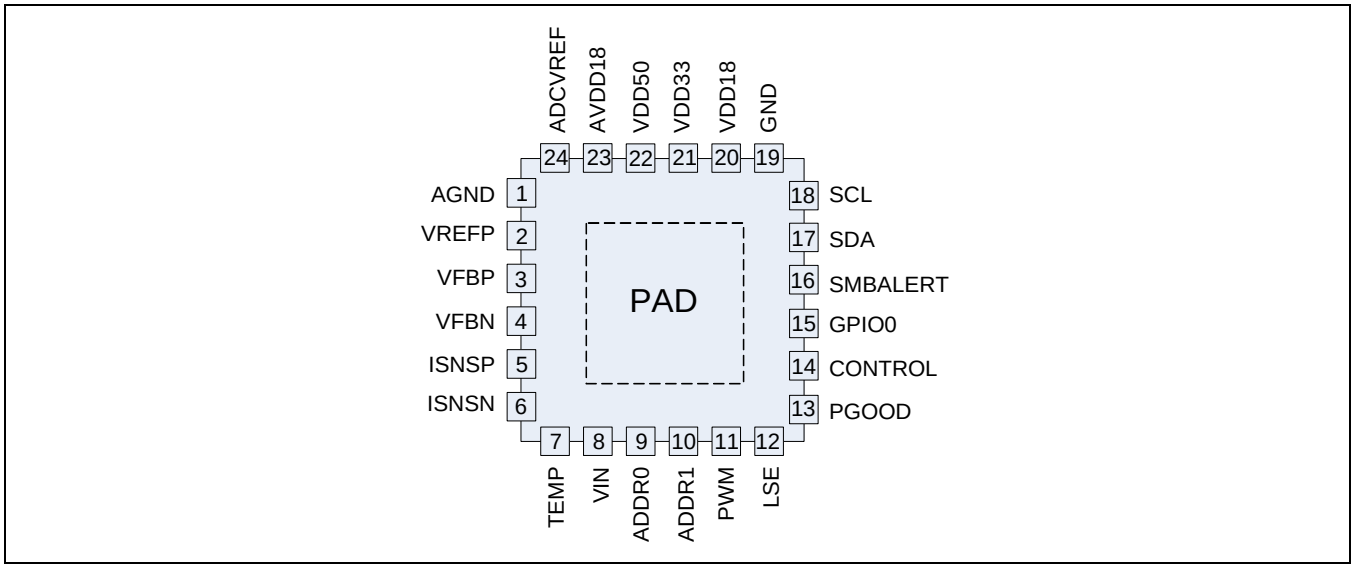
Figure 2.3 Typical Application Circuit with a 5 V Supply Voltage and ZSPM9000



2.4. Available Packages

The ZSPM1000 is available in a 24-pin QFN package. The pin-out is shown in Figure 2.4. The mechanical drawing of the package can be found in Figure 6.1.

Figure 2.4 Pin-Out QFN24 Package



3 Functional Description

3.1. Power Supply Circuitry, Reference Decoupling, and Grounding

The ZSPM1000 incorporates several internal power regulators in order to derive all required supply and bias voltages from a single external supply voltage. This supply voltage can be either 5 V or 3.3 V depending on whether the internal 3.3 V regulator should be used. If the internal 3.3 V regulator is not used, 3.3 V must be supplied to the 3.3 and 5 V supply pins. Decoupling capacitors are required at the VDD33, VDD18, and AVDD18 pins (1.0 µF minimum; 4.7 µF recommended). If the 5.0 V supply voltage is used, i.e. the internal 3.3 V regulator is used, a small load current can be drawn from the VDD33 pin. For example, this can be used to supply pull-up resistors.

The reference voltages required for the analog-to-digital converters are generated within the ZSPM1000. External decoupling must be provided between the VREFP and ADCVREF pins. Therefore, a 4.7 µF capacitor is required at the VREFP pin and a 100 nF capacitor is required at the ADCVREF pin. The two pins should be connected with approximately 50 Ω resistance in order to provide sufficient decoupling between the pins.

Three different ground connections are available on the outside of the package. These should be connected together to a single ground tie. A differentiation between analog and digital ground is not required.

3.2. Reset/Start-up Behavior

The ZSPM1000 employs an internal power-on-reset (POR) circuit to ensure proper start up and shut down with a changing supply voltage. Once the supply voltage increases above the POR threshold voltage, the ZSPM1000 begins the internal start-up process. Upon its completion, the device is ready for operation.

3.3. Digital Power Control

3.3.1. Overview

The digital power control loop consists of the integral parts required for the control functionality of the ZSPM1000. A high-speed analog front-end is used to digitize the output voltage. A digital control core uses the acquired information to provide duty-cycle information to the PWM, which controls the drive signals to the power stage.

3.3.2. Switching Frequency

The ZSPM1000 supports the switching frequencies listed in Table 3.1.

Table 3.1 Supported Switching Frequencies

Supported Switching Frequencies	
1000 kHz	400.0 kHz
800 kHz	333.3 kHz
666.6 kHz	285.7 kHz
571.4 kHz	266.6 kHz
500.0 kHz	222.0 kHz
444.4 kHz	177.0 kHz

3.3.3. Output Voltage Feedback

The voltage feedback signal is sampled with a high-speed analog front-end. The feedback voltage is differentially measured and subtracted from the voltage reference provided by a reference digital-to-analog converter (DAC) using an error amplifier. A flash ADC is then used to convert the voltage into its digital equivalent. This is followed by internal digital filtering to improve the system's noise rejection.

Although the reference DAC generates a voltage up to 1.44 V, keeping the voltage on the feedback pin (VFBP) around 1.20 V is recommended to guarantee sufficient head room. If a larger output voltage is required, an external feedback divider is required.

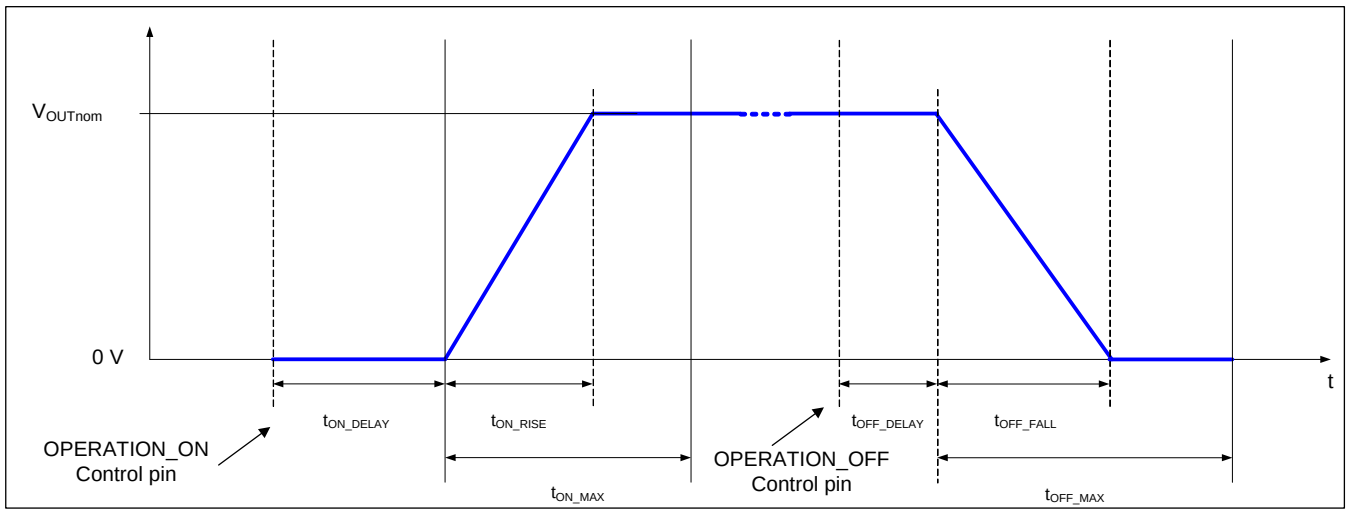
3.3.4. Digital Compensator

Important: *Section 3.3.4 is confidential and requires a non-disclosure agreement (NDA) with ZMDI.*

3.3.5. Power Sequencing and the CONTROL Pin

The ZSPM1000 supports power sequencing features such as programmable ramp up/down and delays. The typical sequence of events is shown in Figure 3.1 and follows the PMBus™ standard. The individual values can be configured using the appropriate configuration setting. Three different configuration options are supported to turn the device on. The device can be configured to turn on immediately after POR, on an OPERATION_ON command, or on an edge on the CONTROL pin.

Figure 3.1 Power Sequencing

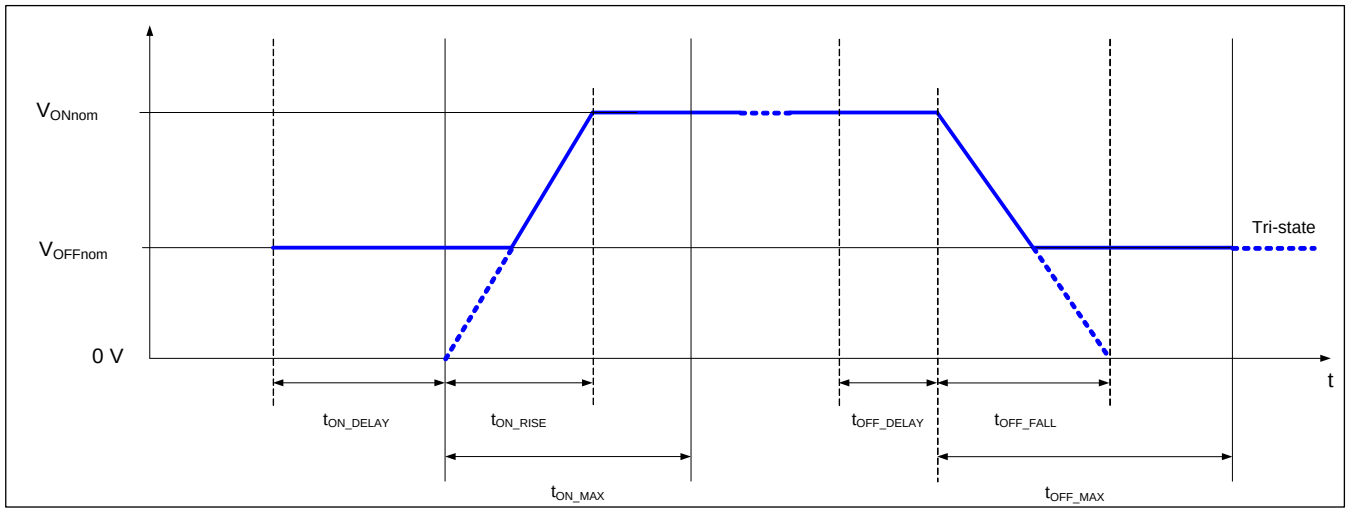


3.3.6. Pre-biased Start-up and Soft Stop

Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this phase.

The ZSPM1000 also supports pre-biased off; i.e., the output voltage is not ramped down to zero and instead remains at a predefined level (V_{OFF_nom}). This value can be configured via the Pink Power Designer™ graphical user interface (GUI). After receiving the shutdown command via PMBus™ or the CONTROL pin, the ZSPM1000 ramps down the value to the predefined value. Once the value is reached, PWM and LSE will be turned off in order to put the output driver into tri-state mode.

Figure 3.2 Power Sequencing with Non-zero Off Voltage



3.3.7. Current Sensing

Important: *Section 3.3.7 is confidential and requires a non-disclosure agreement (NDA) with ZMDI.*

3.3.8. Temperature Measurement

The ZSPM1000 features two independent temperature measurement units. While the internal temperature sensing measures the temperatures inside the ZSPM1000, the external temperature sense element should be placed close to the inductor to measure its temperature. A PN-junction is used as an external temperature sense element. Small-signal transistors, such the 3904, are widely used for this application. The configuration of the sensitivity and the offset is required in the Pink Power Designer™. A temperature calibration is highly recommended.

3.4. Fault Monitoring and Response Generation

The ZSPM1000 monitors various signals during operation. Depending on the selected configuration, it can respond to events generated by these signals. A wide range of options is configurable via the Pink Power Designer™. Typical monitoring within the ZSPM1000 is a three step process. First, an event is generated by a configurable set of thresholds. This event is then digitally filtered before the ZSPM1000 reacts with a configurable response. For most monitored signals, a warning and a fault threshold can be configured. A warning typically sets a status flag, but does not trigger a response, whereas a fault also generates a response.

Each warning and fault event can be individually enabled. The assertion of the SMBALERT signal can also be configured to individual needs. An overview of the options and configuration is given in Table 3.2.

Table 3.2 Fault Configuration Overview

Signal	Fault Level	Response Type	Delay Resolution	Maximum Delay
Output Over-Voltage	Warning			
	Fault	Low impedance	500 µs	90 ms
Output Under-Voltage	Warning			
	Fault	Low-impedance	500 µs	90 ms
Input Over-Voltage	Warning			
	Fault	Off	500 µs	90 ms
Input Under-Voltage	Warning			
	Fault	Off	500 µs	90 ms
Over-Current	Warning			
	Fault	Low-impedance	500 µs	90 ms
External Over-Temperature	Warning			
	Fault	Off	5 ms	900 ms
Internal Over-Temperature	Warning			
	Fault	Off	5 ms	900 ms

The ZSPM1000 supports different response types depending on the fault detected. An “Off” response ramps the output voltage down using the falling-edge sequencer settings. The final state of the output signals depends on the value selected for V_{OFFnom}. The “low-impedance” response turns off the top MOSFET and enables the low-side MOSFET; i.e., PWM=0 and LSE=1.

For each fault response, a delay and a retry setting can be configured. If the delay value is set to non-zero, the ZSPM1000 will not respond to a fault immediately. Instead it will delay the response by the configured value and then reassess the signal. If the fault is still present, the appropriate response will be triggered. If the fault is no longer present, the previous detection will be disregarded. The retry setting configures the number of restarts of the power converter after a fault event. This number can be between zero and seven, where a setting of seven represents an infinite retry operation. In analog controllers, this feature is also known as “hiccup mode.”

3.4.1. Output Over/Under-Voltage

To prevent damage to the load, the ZSPM1000 utilizes an output over-voltage protection circuit. The voltage at VFBP is continuously compared with a configurable threshold using a high-speed analog comparator. If the voltage exceeds the configured threshold, the fault response is generated and the PWM outputs are turned off. The voltage fault level is generated by a 6-bit DAC with a reference voltage of 1.60 V resulting in 25 mV resolution.

Additionally, the output voltage is sampled using the HKADC and continuously compared with an output over-voltage warning threshold. If the output voltage exceeds this threshold, a warning is generated and the preconfigured actions are triggered. The ZSPM1000 also monitors the output voltage with two lower thresholds. If the output voltage is below the under-voltage warning level and above the under-voltage fault level, an output voltage under-voltage warning is triggered. If the output voltage falls below the fault level, a fault event is generated.

3.4.2. Output Current Protection and Limiting

The ZSPM1000 continuously monitors the average inductor current and utilizes this information to protect the power supply against excessive output current. Two different types of protection are configurable independently.

Output current limiting to a configured value is supported by reducing the output voltage. Additionally, the maximum output current warning and fault threshold can be used to shut down the ZSPM1000. Both features can be enabled independently. If the over-current fault threshold is chosen below the limiting threshold, the ZSPM1000 will shut down without going into current limiting mode.

3.4.3. Over-Temperature Protection

The ZSPM1000 monitors internal and external temperature. For each, a warning and a fault level can be configured and an appropriate response can be enabled.

3.5. Pin Configuration

The ZSPM1000 offers a flexible configuration scheme for its digital output pins. This enables using the LSE pin (low-side FET control signal) and GPIO pins (general purpose input/output) with different functions depending on the application requirements. The configuration options are listed in Table 3.3.

Table 3.3 Pin Configuration Overview

Pin	LSE	Thermal shutdown	Driver Disable	Hardwire Option
LSE	Active high		High and low active	High and low active
GPIO		High and low active	High and low active	

In LSE mode, the LSE pin is used as an SMOD signal to actively modulate the low-side FET of the power stage. Alternatively, it can be used as a control signal in order to enable/disable the driver. This signal is deasserted prior to the first switching on the PWM pin and asserted shortly after the last switching event. If the pin is not used in the application, a hardwire option can be used to set the pin to a defined level.

While the GPIO pin supports the driver disable feature, it can also be used as a thermal shutdown input. If the pin is asserted by an external source, e.g., the thermal shutdown flag of a DrMOS, the controller flags an external over-temperature fault and reacts accordingly.

Note that if the GPIO pin is configured as the driver disable, the LSE pin must be configured with the LSE feature.

3.6. Configuration

Important: *Section 3.6 is confidential and requires a non-disclosure agreement (NDA) with ZMDI.*

4 PMBus™ Functionality

4.1. Introduction

The ZSPM1000 supports the PMBus™ protocol to enable the use of configuration, monitoring, and fault management during run-time.

The PMBus™ host controller is connected to the ZSPM1000 via the PMBus™ pins. A dedicated SMBALERT pin is provided to notify the host that new status information is present.

The ZSPM1000 supports packet error correction (PEC) according to the PMBus™ specification.

4.2. Timing and Bus Specification

Figure 4.1 PMBus™ Timing Diagram

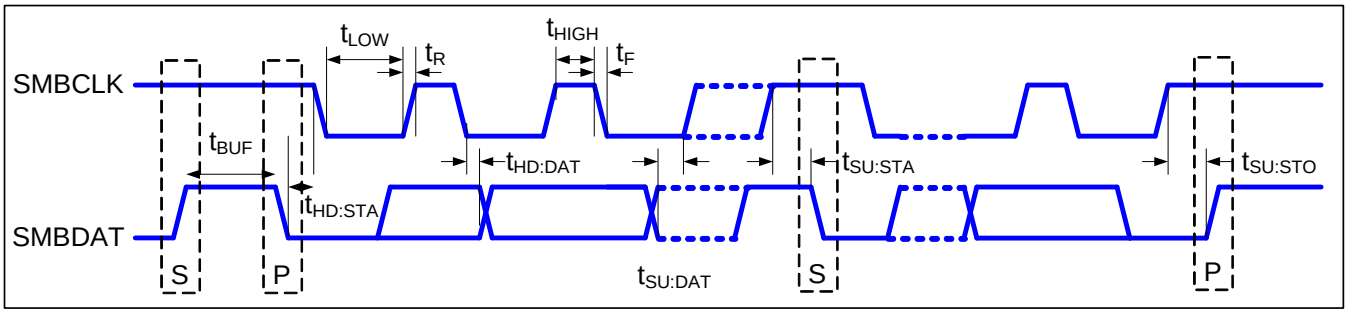


Table 4.1 PMBus™ Timing Specification

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus operation frequency	f_{SMB}		10	400	500	kHz
Bus free time between start and stop	t_{BUF}		1.3			Ms
Hold time after start condition	$t_{HD:STA}$		0.6			Ms
Repeat start condition setup time	$t_{SU:STA}$		0.6			Ms
Stop condition setup time	$t_{SU:STO}$		0.6			Ms
Data hold time	$t_{HD:DAT}$		300			Ns
Data setup time	$t_{SU:DAT}$		100			Ns
Clock low time-out	$t_{TIMEOUT}$			25	35	Ms
Clock low period	t_{LOW}		1.3			Ms
Clock high period	t_{HIGH}		0.6			Ms
Cumulative clock low extend time	$t_{LOW:SEXT}$				25	Ms
Clock or data fall time	t_F				300	Ns
Clock or data rise time	t_R				300	Ns

4.3. Address Selection via External Resistors

PMBus™ uses a 7-bit device address to identify different devices connected to the bus. This address can be selected via external resistors connected to the ADDRx pins.

The resistor values are sensed using the internal ADC during the initialization phase and the appropriate PMBus™ address is selected. Note that the respective circuitry is only active during the initialization phase; hence no DC voltage can be measured at the pins. The supported PMBus™ addresses and the values of the respective required resistors are listed in Table 4.2.

Table 4.2 Supported Resistor Values for PMBus™ Address Selection

Address (Hex)	ADDR1 Ω	ADDR0 Ω	Address (Hex)	ADDR1 Ω	ADDR0 Ω	Address (Hex)	ADDR1 Ω	ADDR0 Ω	Address (Hex)	ADDR1 Ω	ADDR0 Ω
0	0	0	32	1.2 k	0	64	2.7 k	0	96	4.7 k	0
1*	0	680	33	1.2 k	680	65	2.7 k	680	97*	4.7 k	680
2*	0	1.2 k	34	1.2 k	1.2 k	66	2.7 k	1.2 k	98	4.7 k	1.2 k
3*	0	1.8 k	35	1.2 k	1.8 k	67	2.7 k	1.8 k	99	4.7 k	1.8 k
4*	0	2.7 k	36	1.2 k	2.7 k	68	2.7 k	2.7 k	100	4.7 k	2.7 k
5*	0	3.9 k	37	1.2 k	3.9 k	69	2.7 k	3.9 k	101	4.7 k	3.9 k
6*	0	4.7 k	38	1.2 k	4.7 k	70	2.7 k	4.7 k	102	4.7 k	4.7 k
7*	0	5.6 k	39	1.2 k	5.6 k	71	2.7 k	5.6 k	103	4.7 k	5.6 k
8*	0	6.8 k	40*	1.2 k	6.8 k	72	2.7 k	6.8 k	104	4.7 k	6.8 k
9	0	8.2 k	41	1.2 k	8.2 k	73	2.7 k	8.2 k	105	4.7 k	8.2 k
10	0	10 k	42	1.2 k	10 k	74	2.7 k	10 k	106	4.7 k	10 k
11	0	12 k	43	1.2 k	12 k	75	2.7 k	12 k	107	4.7 k	12 k
12*	0	15 k	44	1.2 k	15 k	76	2.7 k	15 k	108	4.7 k	15 k
13	0	18 k	45	1.2 k	18 k	77	2.7 k	18 k	109	4.7 k	18 k
14	0	22 k	46	1.2 k	22 k	78	2.7 k	22 k	110	4.7 k	22 k
15	0	27 k	47	1.2 k	27 k	79	2.7 k	27 k	111	4.7 k	27 k
16	680	0	48	1.8 k	0	80	3.9 k	0	112	5.6 k	0
17	680	680	49	1.8 k	680	81	3.9 k	680	113	5.6 k	680
18	680	1.2 k	50	1.8 k	1.2 k	82	3.9 k	1.2 k	114	5.6 k	1.2 k
19	680	1.8 k	51	1.8 k	1.8 k	83	3.9 k	1.8 k	115	5.6 k	1.8 k
20	680	2.7 k	52	1.8 k	2.7 k	84	3.9 k	2.7 k	116	5.6 k	2.7 k
21	680	3.9 k	53	1.8 k	3.9 k	85	3.9 k	3.9 k	117	5.6 k	3.9 k
22	680	4.7 k	54	1.8 k	4.7 k	86	3.9 k	4.7 k	118	5.6 k	4.7 k
23	680	5.6 k	55*	1.8 k	5.6 k	87	3.9 k	5.6 k	119	5.6 k	5.6 k
24	680	6.8 k	56	1.8 k	6.8 k	88	3.9 k	6.8 k	120*	5.6 k	6.8 k
25	680	8.2 k	57	1.8 k	8.2 k	89	3.9 k	8.2 k	121*	5.6 k	8.2 k
26	680	10 k	58	1.8 k	10 k	90	3.9 k	10 k	122*	5.6 k	10 k
27	680	12 k	59	1.8 k	12 k	91	3.9 k	12 k	123*	5.6 k	12 k
28	680	15 k	60	1.8 k	15 k	92	3.9 k	15 k	124*	5.6 k	15 k
29	680	18 k	61	1.8 k	18 k	93	3.9 k	18 k	125*	5.6 k	18 k
30	680	22 k	62	1.8 k	22 k	94	3.9 k	22 k	126*	5.6 k	22 k
31	680	27 k	63	1.8 k	27 k	95	3.9 k	27 k	127*	5.6 k	27 k

Note: * These addresses are reserved by the SMBus specification.

If only four devices are used in a system, their respective addresses can alternatively be configured without resistors by connecting the pins to GND or AVDD18 pin. The PMBus™ addresses selectable in this fashion are listed in Table 4.3.

Table 4.3 PMBus™ Address Selection without Resistors

Address	ADDR1	ADDR0
15	GND	AVDD18
48	AVDD18	GND
63	AVDD18	AVDD18
64	GND	GND

4.4. Configuration

Important: *Section 4.4 is confidential and requires a non-disclosure agreement (NDA) with ZMDI.*

4.5. Monitoring

The ZSPM1000 has a dedicated set of PMBus™ registers to enable advanced power management using extensive monitoring features. Different warning and error flags can be read by the PMBus™ master to ensure proper operation of the power converter or monitor the converters over its life time.

Important: *The subsequent table in this section is confidential and requires a non-disclosure agreement (NDA) with ZMDI.*

4.6. Miscellaneous

Important: *Section 4.6 is confidential and requires a non-disclosure agreement (NDA) with ZMDI.*

4.7. Detailed Description of the Supported PMBus™ Commands

Important: *Section 4.7 is confidential and requires a non-disclosure agreement (NDA) with ZMDI.*

5 External Component Selection

5.1. Output Voltage Feedback Components

Important: *Section 5.1 is confidential and requires a non-disclosure agreement (NDA) with ZMDI.*

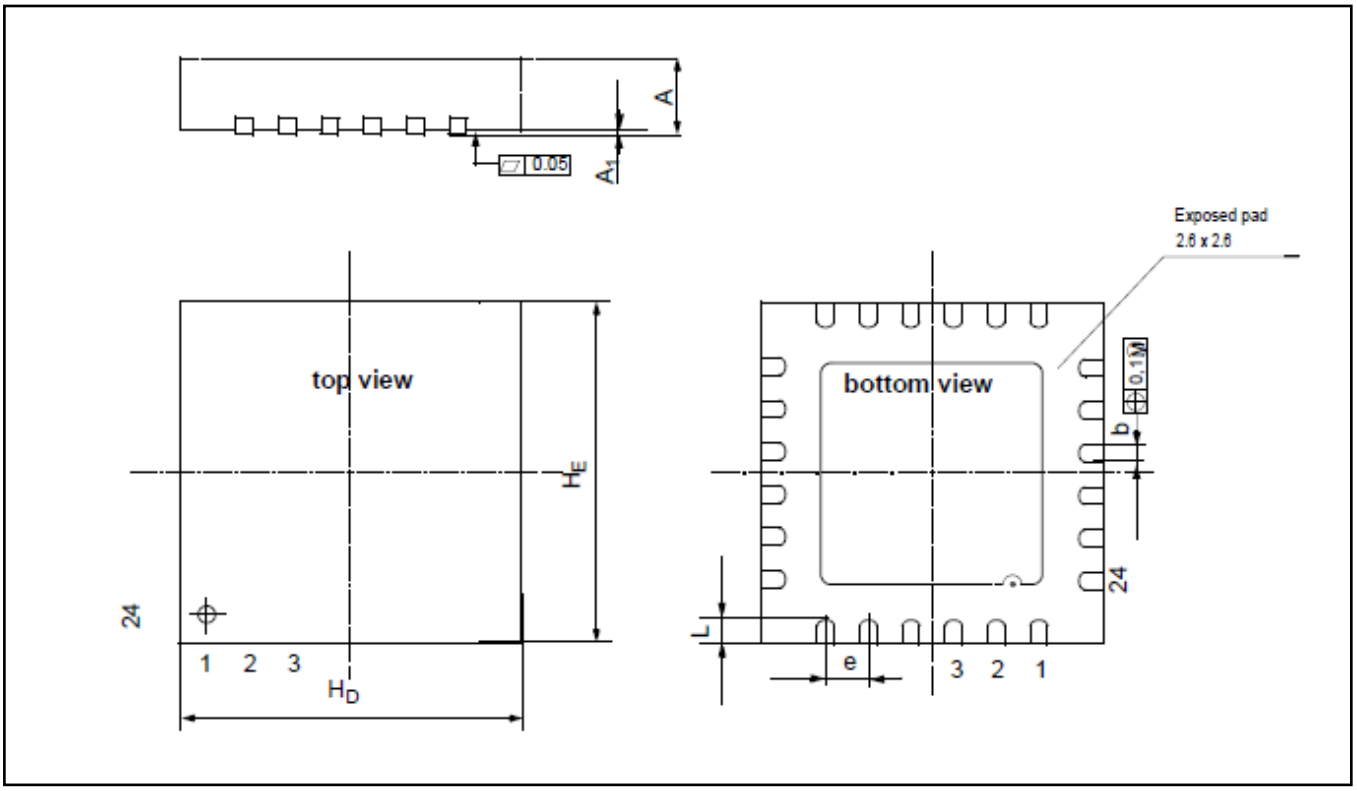
5.2. DCR Current Sensing Components

Important: *Sections 5.2 and 5.3 are confidential and require a non-disclosure agreement (NDA) with ZMDI.*

6 Mechanical Specifications

Based on JEDEC MO-220. All dimensions are in millimeters.

Figure 6.1 Package Drawing



Dimensions [mm]	Min	Max
A	0.8	0.90
A_1	0.00	0.05
b	0.18	0.30
e	0.5 nominal	
H_D	3.90	4.1
H_E	3.90	4.1
L	0.35	0.45

7 Ordering Information

Product Sales Code	Description	Package
ZSPM1000ZI1R 1	ZSPM1000 Lead-free QFN24 — Temperature range: -40°C to +85°C	Reel
ZSPM1000ZI1R 0	ZSPM1000 lead-free QFN24 without Power-One® licensing fee[†] Temperature range: -40°C to +85°C	Reel
ZSPM1000ZA1R 1	ZSPM1000 Lead-free QFN24 — Temperature range: -40°C to +125°C	Reel
ZSPM1000ZA1R 0	ZSPM1000 lead-free QFN24 without Power-One® licensing fee[‡] Temperature range: -40°C to +125°C	Reel
ZSPM8000-KIT	Evaluation Kit for ZSPM1000 including PMBus™ Communication Interface and Pink Power Designer™ Software	Kit

8 Related Documents

Note: *X_xy* refers to the current revision of the document.

Document	File Name
ZSPM8000-KIT Evaluation Kit Description	*ZSPM8000_Eval_Kit_Rev_X_xy.pdf*
Pink Power Designer™ Graphic User Interface (GUI)	*UserGUIDE_Rev_X_xy.pdf*

Visit ZMDI's website www.zmdi.com or contact your nearest sales office for the latest version of these documents.

9 Glossary

Term	Description
ASIC	Application Specific Integrated Circuit
DPWM	Digital Pulse-Width Modulator
DSP	Digital Signal Processing
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
HKADC	Housekeeping Analog-To-Digital Converter
NVM	Non-volatile Memory
OT	Over-Temperature
OTP	One-Time Programmable Memory
OV	Over-Voltage
SCR	Sub-cycle Response™
SLC	State-Law Control™

[†] Power-One® is a trademark of Power-One, Inc.
[‡] Power-One® is a trademark of Power-One, Inc.

Term	Description
SMOD	Skip Mode
SPM	Smart Power Management

10 Document Revision History

Revision	Date	Description
1.41	April 24, 2013	First release of brief data sheet.

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