



Integrated Device Technology, Inc.

# FAST CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT373/2373T/AT/CT/DT  
IDT54/74FCT533/2533T/AT/CT  
IDT54/74FCT573/2573T/AT/CT/DT

## FEATURES:

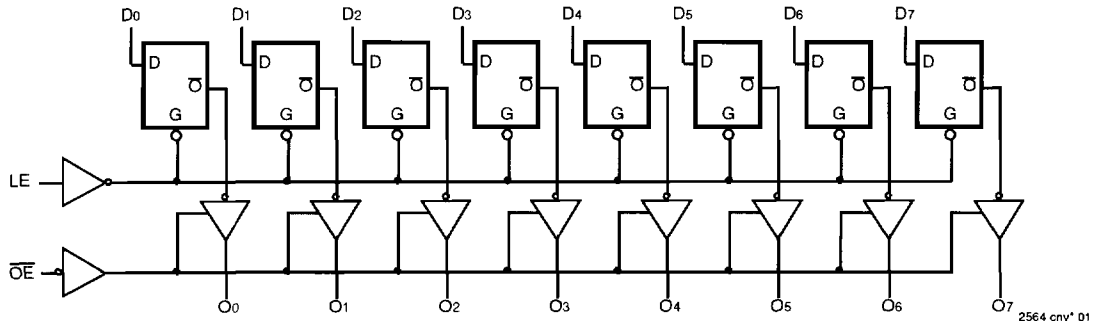
- **Common features:**
  - Std., A, C and D speed grades
  - Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - $V_{OH} = 3.3\text{V}$  (typ.)
    - $V_{OL} = 0.3\text{V}$  (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT373T/533T/573T:**
  - High drive outputs (-15mA  $I_{OH}$ , 48mA  $I_{OL}$ )
  - Power off disable outputs permit "live insertion"
- **Features for FCT2373T/2533T/2573T:**
  - Balanced Output Drivers:  $\pm 24\text{mA}$  (commercial),  $\pm 16\text{mA}$  (military)
  - Reduced system switching noise

## DESCRIPTION:

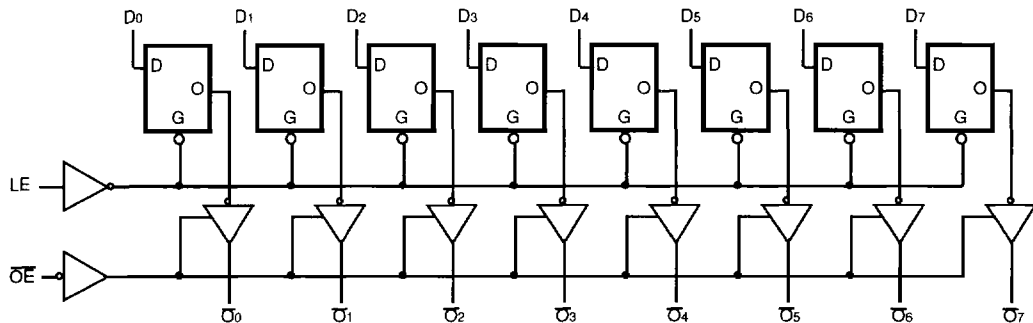
The IDT54/74FCT373/2373T/AT/CT/DT, IDT54/74FCT533/2533T/AT/CT and IDT54/74FCT573/2573T/AT/CT/DT are octal transparent latches built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the bus output is in the high-impedance state.

The IDT54/74FCT2373T/AT/CT/DT, IDT54/74FCT2533T/AT/CT and IDT54/74FCT2573T/AT/CT/DT have balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The IDT54/74FCT2xxxT parts are plug-in replacements for IDT54/74FCTxxxT parts.

## FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT373T/2373T AND IDT54/74FCT573T/2573T



## FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT533T/2533T



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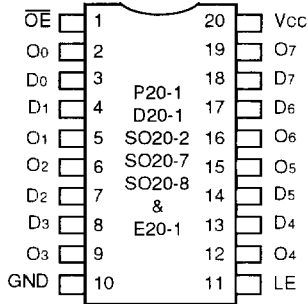
2564 cnv\* 02

MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

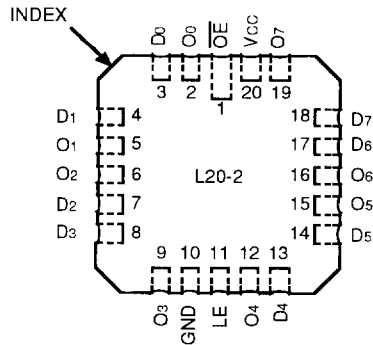
**PIN CONFIGURATIONS**

**IDT54/74FCT373/2373T**



**DIP/SOIC/SSOP/QSOP/CERPACK  
 TOP VIEW**

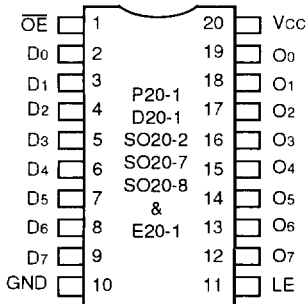
2564 cnv\* 03



**LCC  
 TOP VIEW**

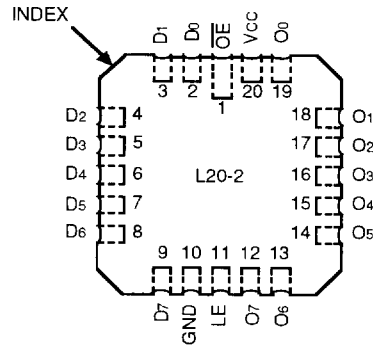
2564 cnv\* 04

**IDT54/74FCT573/2573T**



**DIP/SOIC/SSOP/QSOP/CERPACK  
 TOP VIEW**

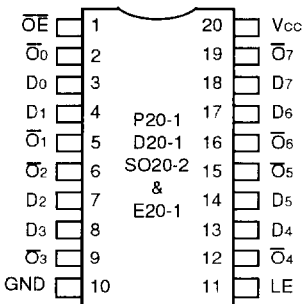
2564 cnv\* 05



**LCC  
 TOP VIEW**

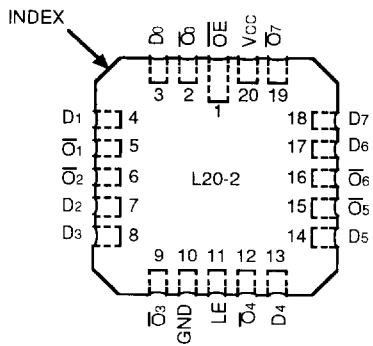
2564 cnv\* 06

**IDT54/74FCT533/2533T**



**DIP/SOIC/CERPACK  
 TOP VIEW**

2564 cnv\* 07



**LCC  
 TOP VIEW**

2564 cnv\* 08



**FUNCTION TABLE (533)<sup>(1)</sup>**

Inputs			Outputs
DN	LE	OE	ON
H	H	L	L
L	H	L	H
X	X	H	Z

**NOTE:**

1. H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 Z = High Impedance

2564 tbl 01

**FUNCTION TABLE (373 and 573)<sup>(1)</sup>**

Inputs			Outputs
DN	LE	OE	ON
H	H	L	H
L	H	L	L
X	X	H	Z

**NOTE:**

1. H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 Z = High Impedance

2564 tbl 02

**DEFINITION OF FUNCTIONAL TERMS**

Pin Names	Description
DN	Data Inputs
LE	Latch Enable Input (Active HIGH)
OE	Output Enable Input (Active LOW)
ON	3-State Outputs
ON	Complementary 3-State Outputs

2564 tbl 03

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	-60 to +120	-60 to +120	mA

**NOTES:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.  
 2. Input and V<sub>CC</sub> terminals only  
 3. Outputs and I/O terminals only.

2564 lmk 04

**CAPACITANCE** (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**NOTE:**

1. This parameter is measured at characterization but not tested.

2564 lmk 05

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; Military:  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ $V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(4)</sup>		$V_I = 0.5\text{V}$	—	—	
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(4)</sup>	$V_{CC} = \text{Max.}$ $V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = 0.5\text{V}$	—	—	
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$	—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$	-60	-120	-225	mA
$V_H$	Input Hysteresis	—	—	200	—	mV
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or $V_{CC}$	—	0.01	1	mA

2564 Ink 06

## OUTPUT DRIVE CHARACTERISTICS FOR FCT373T/533T/573T

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -6\text{mA MIL.}$	2.4	3.3	—	V
			$I_{OH} = -8\text{mA COM'L.}$	—	—	—	—
		$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	—	0.3	0.5	V	
$I_{OFF}$	Input/Output Power Off Leakage <sup>(6)</sup>	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$	

2564 Ink 07

## OUTPUT DRIVE CHARACTERISTICS FOR FCT2373T/2533T/2573T

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$I_{ODL}$	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$	60	115	150	mA	
$I_{ODH}$	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$	-60	-115	-150	mA	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -16\text{mA MIL.}$	2.4	3.3	—	V
			$I_{OH} = -24\text{mA COM'L.}$	—	—	—	—
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	—	0.3	0.55	V	

2564 Ink 08

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}, +25^\circ\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .
- This parameter is guaranteed but not tested.

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**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>			Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>			—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub>	FCTxxxT	—	0.15	0.25	mA/ MHz
			V <sub>IN</sub> = GND	FCT2xxxT	—	0.06	0.12	
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub>	FCTxxxT	—	1.5	3.5	mA
			V <sub>IN</sub> = GND	FCT2xxxT	—	0.6	2.2	
			V <sub>IN</sub> = 3.4	FCTxxxT	—	1.8	4.5	
			V <sub>IN</sub> = GND	FCT2xxxT		0.9	3.2	
			V <sub>IN</sub> = V <sub>CC</sub>	FCTxxxT	—	3.0	6.0 <sup>(5)</sup>	
			V <sub>IN</sub> = GND	FCT2xxxT	—	1.2	3.4 <sup>(5)</sup>	
		V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V <sub>CC</sub> Eight Bits Toggling	V <sub>IN</sub> = 3.4	FCTxxxT	—	5.0	14.0 <sup>(5)</sup>	
			V <sub>IN</sub> = GND	FCT2xxxT	—	3.2	11.4 <sup>(5)</sup>	

**NOTES:**

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V). All other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 I<sub>C</sub> = I<sub>CC</sub> +  $\Delta I_{CC} DHNT$  + I<sub>CCD</sub> (f<sub>CP</sub>/2 + f<sub>i</sub>N<sub>i</sub>)  
 I<sub>CC</sub> = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 DH = Duty Cycle for TTL Inputs High  
 NT = Number of TTL Inputs at DH  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT373T/573T FCT2373T/2573T				FCT373AT/573AT FCT2373AT/2573AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	ns
tsu	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	ns

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Symbol	Parameter	Conditions <sup>(1)</sup>	FCT373CT/573CT FCT2373CT/2573CT				FCT373DT/573DT FCT2373DT/2573DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	4.2	1.5	5.1	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	5.5	2.0	8.0	2.0	4.0	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.5	1.5	6.3	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.0	1.5	5.9	1.5	4.0	—	—	ns
tsu	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	1.5	—	—	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.0	—	—	—	ns
tw	LE Pulse Width HIGH <sup>(3)</sup>		5.0	—	6.0	—	3.0	—	—	—	ns

**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

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**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT533T FCT2533T				FCT533AT FCT2533AT				FCT533CT FCT2533CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to ON		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t <sub>w</sub>	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

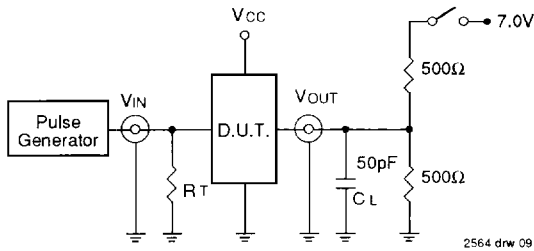
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2564 tbl 12

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

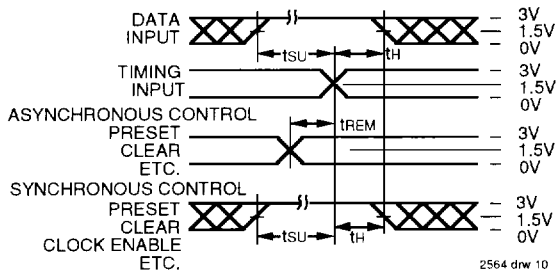
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

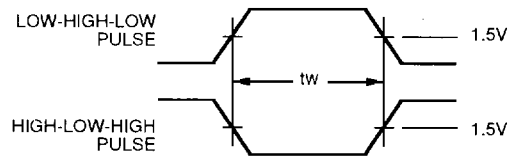
CL = Load capacitance: includes jig and probe capacitance.  
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2564 lrk 13

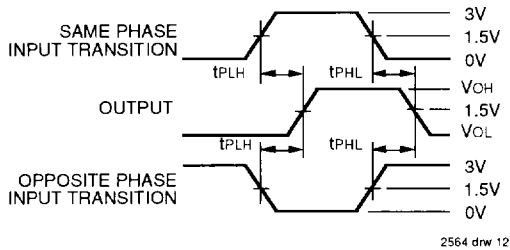
### SET-UP, HOLD AND RELEASE TIMES



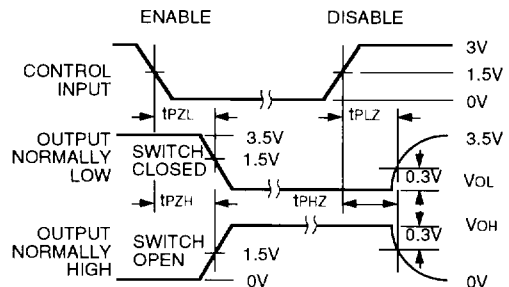
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

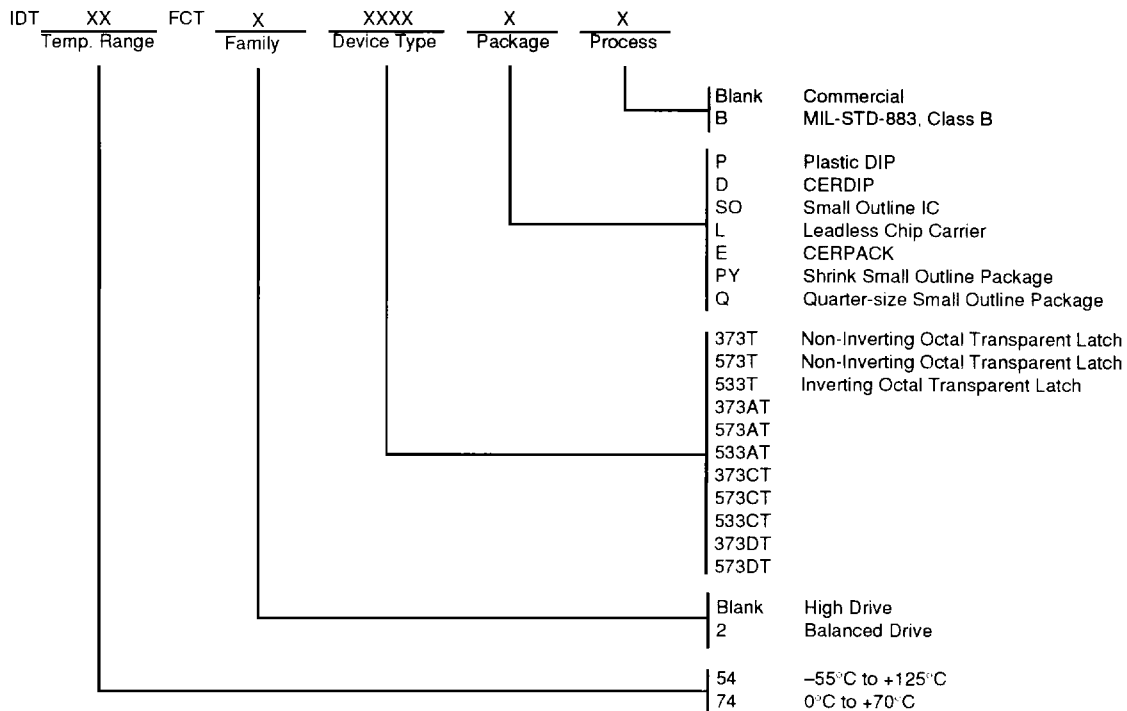


#### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $t_F \leq$  2.5ns;  $t_R \leq$  2.5ns



**ORDERING INFORMATION**



2564 drw 14