National Semiconductor

DM54LS78A/DM74LS78A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Common Clear, Common Clock and Complementary Outputs

General Description

This device contains two negative-edge triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

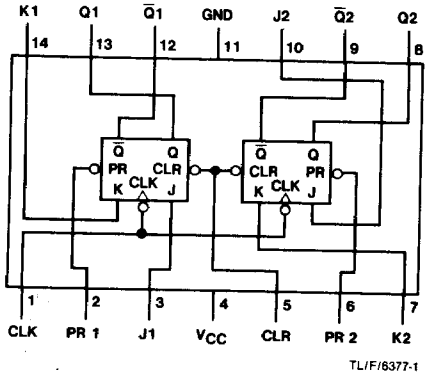
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6377-1

DM54LS78A (J) DM74LS78A (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_O	$\bar{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\bar{Q}_O$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative Going Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM54LS78A			DM74LS78A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	

Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.2	
			Preset			0.2	
			Clock			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			120	
			Preset			60	
			Clock			160	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 4)	J, K			−0.4	mA
			Clear			−1.6	
			Preset			−0.8	
			Clock			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	45		25	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		11	20		21	28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.