FAIRCHILD SEMICONDUCTOR™

May 1998

74ACQ573 • 74ACTQ573
Quiet Series™ Octal Latch with 3-STATE Outputs

General Description

The ACQ/ACTQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The ACQ/ACTQ573 is functionally identical to the ACQ/ACTQ373 but with inputs and outputs on opposite sides of the package. The ACQ/ACTQ utilizes Fairchild's Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

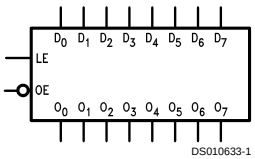
- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Outputs source/sink 24 mA
- Faster prop delays than standard AC/ACT573
- 4 kV minimum ESD immunity

Ordering Code:

Order Number	Package Number	Package Description
74ACQ573SC	M20B	20-Lead (0.300" Wide) Molded Small Outline Package
74ACQ573SJ	M20D	20-Lead (0.300" Wide) Molded Shrink Small Outline Package EIAJ
74ACQ573PC	V20A	20-Lead Molded Dual-in-Line Package
74ACTQ573SC	M20B	20-Lead (0.300" Wide) Molded Small Outline Package
74ACTQ573SJ	M20D	20-Lead (0.300" Wide) Molded Shrink Small Outline Package EIAJ
74ACTQ573PC	V20A	20-Lead Molded Dual-in-Line Package
74ACTQ573QSC	MQA20	20-Lead (0.150" Wide) Molded Shrink Small Outline Package

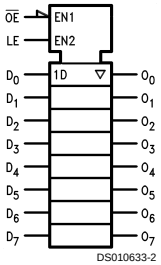
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



DS010633-1

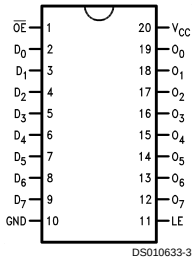
IEEE/IEC



DS010633-2

Connection Diagram

Pin Assignment for DIP QSOP and SOIC



DS010633-3

Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3-STATE Output Enable Input
O_0–O_7	3-STATE Latch Outputs

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Truth Table

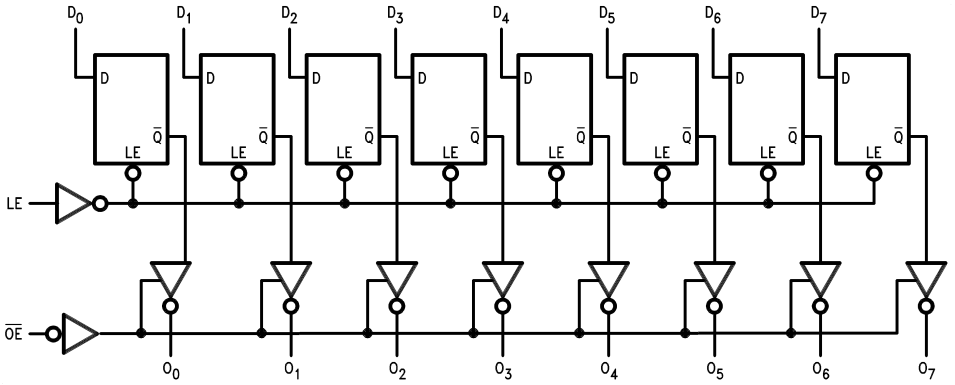
Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Functional Description

The ACQ/ACTQ573 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D-type input changes. When LE is LOW the latches store the information that was present on the D-type inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



DS010633-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
DC Latchup Source or Sink Current	±300 mA
Junction Temperature (T_J) PDIP	140˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
ACQ	2.0V to 6.0V
ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40˚C to +85˚C
Minimum Input Edge Rate ΔV/Δt	
ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt	
ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V)	T_A = +25˚C	T_A = −40˚C to +85˚C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 µA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		I_{OH} = −12 mA
		4.5		3.86	3.76		I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 µA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44		I_{OL} = 12 mA
		4.5		0.36	0.44		I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	µA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	V_{OLD} = 1.65 V_{Max}
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85 V_{Min}
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	µA	V_{IN} = V_{CC} or GND
I_{OZ}	Maximum 3-STATE Leakage Curent	5.5		±0.25	±2.5	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
V_{OLP}	Quiet Output	5.0	1.1	1.5		V	*Figures 1, 2*

DC Electrical Characteristics for ACQ (Continued)

Symbol	Parameter	V_{CC} (V)	T_A = +25˚C		T_A = −40˚C to +85˚C	Units	Conditions
			Typ	Guaranteed Limits			
	Maximum Dynamic V_{OL}						(Notes 5, 6)
V_{OLV}	Quiet Output	5.0	−0.6	−1.2		V	*Figures 1, 2*
	Minimum Dynamic V_{OL}						(Notes 5, 6)
V_{IHD}	Minimum High Level	5.0	3.1	3.5		V	(Notes 5, 7)
	Dynamic Input Voltage						
V_{ILD}	Maximum Low Level	5.0	1.9	1.5		V	(Notes 5, 7)
	Dynamic Input Voltage						

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 5: Plastic DIP package.

Note 6: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 7: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V)	T_A = +25˚C		T_A = −40˚C to +85˚C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	0.8	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 µA
	Output Voltage	5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 8)
V_{OL}	Maximum Low Level	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 µA
	Output Voltage	5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 8)
I_{IN}	Maximum Input	5.5		±0.1	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current						
I_{OZ}	Maximum 3-STATE	5.5		±0.25	±2.5	µA	V_I = V_{IL}, V_{IH}
	Leakage Current						V_O = V_{CC}, GND
I_{CCT}	Maximum	5.5	0.6		1.5	mA	V_I = V_{CC} − 2.1V
	I_{CC}/Input						
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 9)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5		4.0	40.0	µA	V_{IN} = V_{CC}
	Supply Current						or GND
V_{OLP}	Quiet Output	5.0	1.1	1.5		V	*Figures 1, 2*
	Maximum Dynamic V_{OL}						(Notes 10, 11)
V_{OLV}	Quiet Output	5.0	−0.6	−1.2		V	*Figures 1, 2*
	Minimum Dynamic V_{OL}						(Notes 10, 11)
V_{IHD}	Minimum High Level	5.0	1.9	2.2		V	(Notes 10, 12)
	Dynamic Input Voltage						

DC Electrical Characteristics for ACTQ (Continued)

Symbol	Parameter	V_{CC} (V)	T_A = +25°C		T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Notes 10, 12)

Note 8: All outputs loaded; thresholds on input associated with output under test.

Note 9: Maximum test duration 2.0 ms, one output loaded at a time.

Note 10: Plastic DIP package.

Note 11: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 12: Max number of data inputs (n) switching. (n − 1) inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f =1 MHz.

AC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V) (Note 13)	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL}	Propagation Delay	3.3	2.5	8.5	10.5	2.5	11.0	ns
t_{PLH}	D_n to O_n	5.0	1.5	5.5	7.0	1.5	7.5	
t_{PLH}	Propagation Delay	3.3	2.5	8.5	12.0	2.5	12.5	ns
t_{PHL}	LE to O_n	5.0	2.0	6.0	8.0	2.0	8.5	
t_{PZL}	Output Enable Time	3.3	2.5	8.5	13.0	2.5	13.5	ns
t_{PZH}		5.0	1.5	6.0	8.5	1.5	9.0	
t_{PHZ}	Output Disable Time	3.3	1.0	9.0	14.5	1.0	15.0	ns
t_{PLZ}		5.0	1.0	6.0	9.5	1.0	10.0	
t_{OSHL}	Output to Output Skew (Note 14)	3.3		1.0	1.5		1.5	ns
t_{OSLH}	D_n to O_n	5.0		0.5	1.0		1.0	

Note 13: VoltageRange 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL} or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 15)	T_A = +25°C, C_L = 50 pF		T_A = −40°C to +85°C, C_L = 50 pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW	3.3	0	3.0	3.0	ns
	D_n to LE	5.0	0	3.0	3.0	
t_H	Hold Time, HIGH or LOW	3.3	0	1.5	1.5	ns
	D_n to LE	5.0	0	1.5	1.5	
t_W	LE Pulse Width, HIGH	3.3	2.0	4.0	4.0	ns
		5.0	2.0	4.0	4.0	

Note 15: Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

AC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V) (Note 16)	$T_A = +25^\circ C$, $C_L = 50$ pF			$T_A = -40^\circ C$ to $+85^\circ C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay D_n to O_n	5.0	2.0	6.5	7.5	2.0	8.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	7.0	8.5	2.5	9.0	ns
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.0	9.0	2.0	9.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.0	10.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 17) D_n to O_n	5.0		0.5	1.0		1.0	ns

Note 16: Voltage Range 5.0 is 5.0V ±0.5V

Note 17: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL} or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements for ACTQ

Symbol	Parameter	V_{CC} (V) (Note 18)	$T_A = +25^\circ C$, $C_L = 50$ pF		$T_A = -40^\circ C$ to $+85^\circ C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW D_n to LE	5.0	0	3.0	3.0	ns
t_H	Hold Time, HIGH or LOW D_n to LE	5.0	0	1.5	1.5	ns
t_W	LE Pulse Width, HIGH	5.0	2.0	4.0	4.0	ns

Note 18: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	42.0	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator

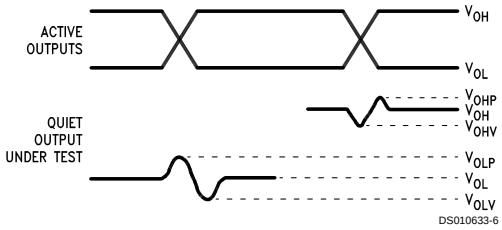
PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

FACT Noise Characteristics (Continued)



Note 19: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note 20: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

FIGURE 1. Quiet Output Noise Voltage Waveforms

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output durnig the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

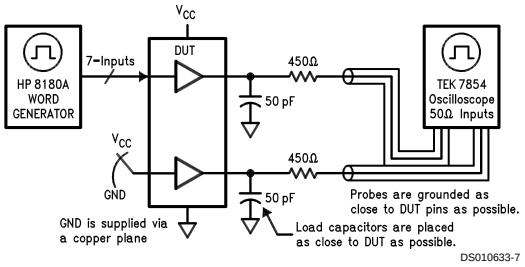
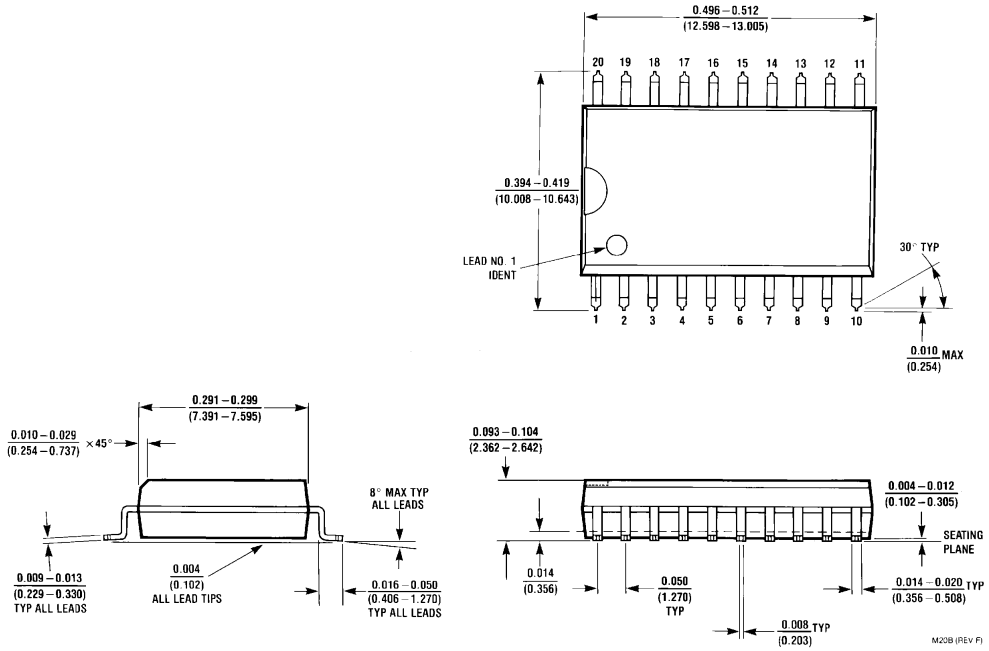
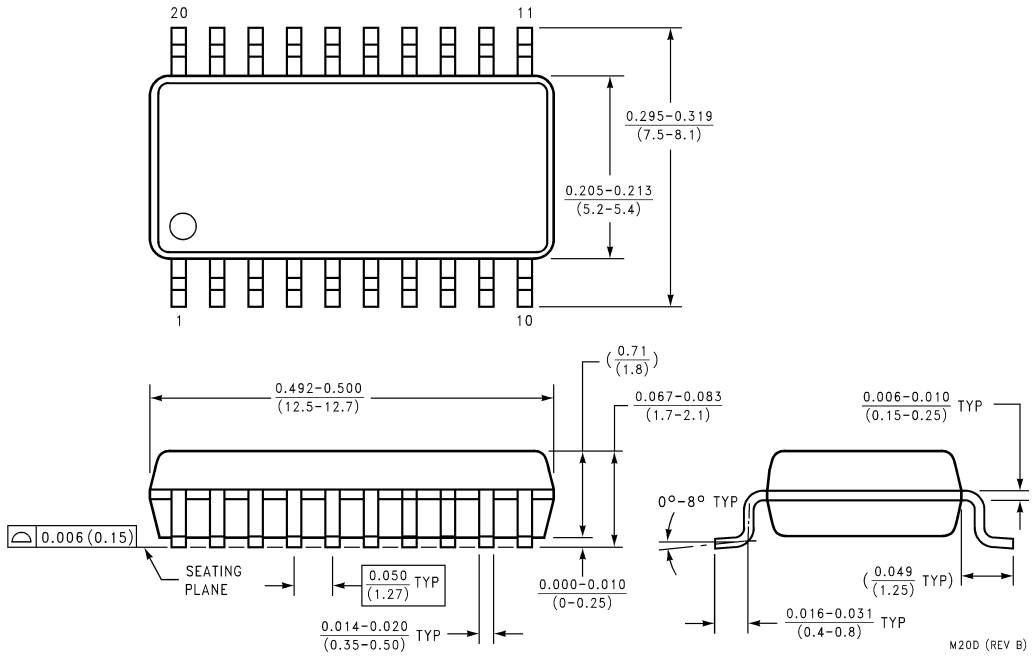


FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted

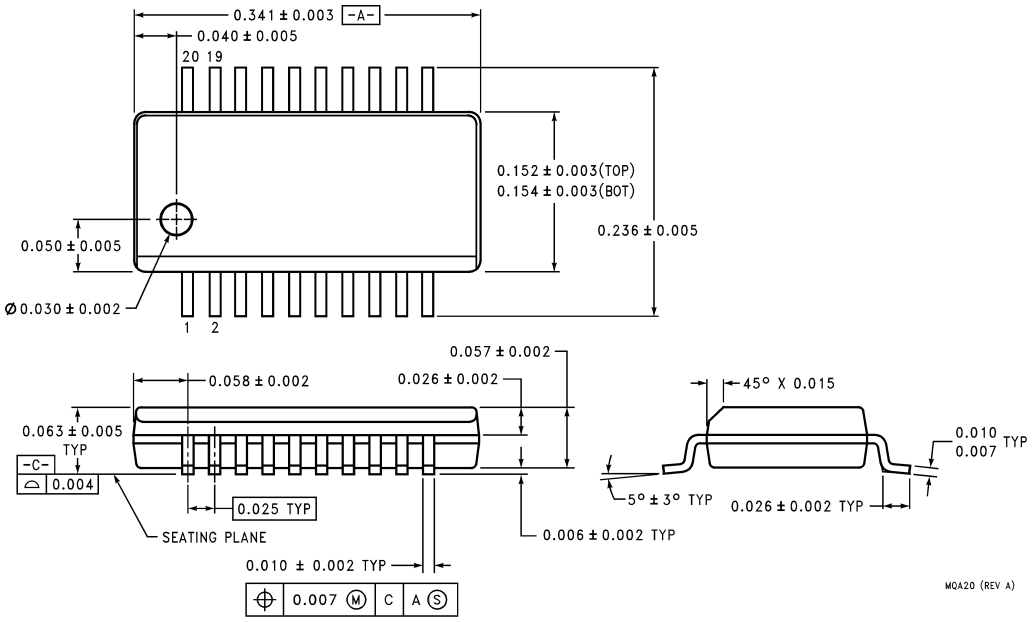


20-Lead (0.300" Wide) Molded Small Outline Package
Package Number M20B

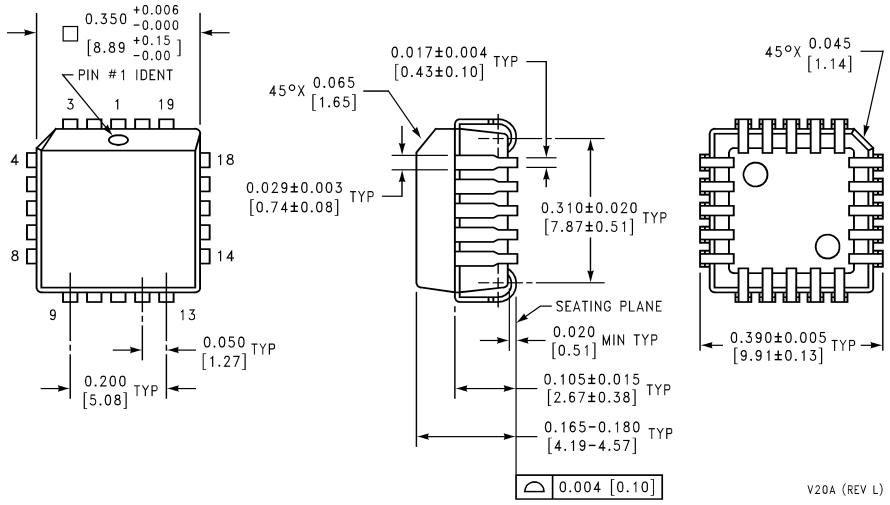


20-Lead (0.300" Wide) Molded Shrink Small Outline Package EIAJ
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead (0.150" Wide) Molded Shrink Small Outline Package
Package Number MQA20



20-Lead Molded Dual-in-Line Package
Package Number V20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372
Fax: 972-910-8036

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
8/F Room 808 Empire Centre
68 Mody Road, Tsimshatsui East
Kowloon, Hong Kong
Tel: 852-2722-8338
Fax: 852-2722-8383

Fairchild Semiconductor Japan Ltd.
4F, Natsume BI,
2-18-6 Yushima, Bunkyo-ku,
Tokyo 113-0034, Japan
Tel: 81-3-3818-8840
Fax: 81-3-3818-8450

www.fairchildsemi.com