

SN54F11, SN74F11 TRIPLE 3-INPUT POSITIVE-AND GATES

SDFS040A – MARCH 1987 – REVISED OCTOBER 1993

- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

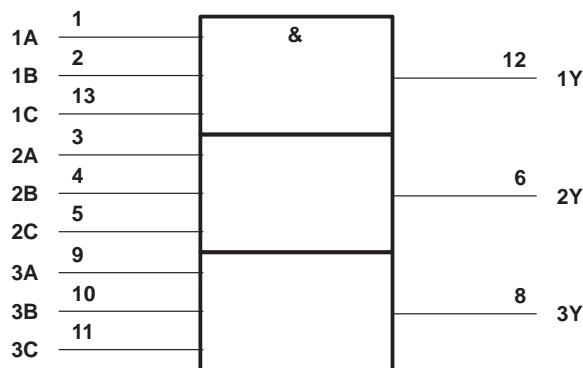
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \bar{A} + \bar{B} + \bar{C}$ in positive logic.

The SN54F11 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F11 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

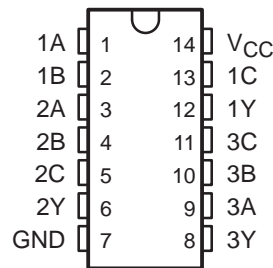
logic symbol†



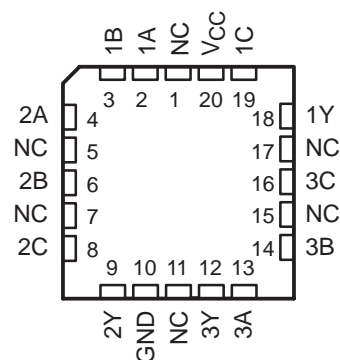
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

SN54F11 ... J PACKAGE
SN74F11 ... D OR N PACKAGE
(TOP VIEW)

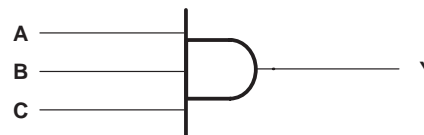


SN54F11 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram, each gate (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the high state	–0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F11	–55°C to 125°C
SN74F11	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F11			SN74F11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–1			–1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F11			SN74F11			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.5	3.4		2.5	3.4		V
	$V_{CC} = 4.75$ V, $I_{OH} = -1$ mA				2.7			
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA		0.3	0.5		0.3	0.5	V
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			20	μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.5$ V			–0.6			–0.6	mA
$I_{OS}§$	$V_{CC} = 5.5$ V, $V_O = 0$	–60		–150	–60		–150	mA
I_{CCH}	$V_{CC} = 5.5$ V, $V_I = 4.5$ V		4.1	6.2		4.1	6.2	mA
I_{CCL}	$V_{CC} = 5.5$ V, $V_I = 0$		6.5	9.7		6.5	9.7	mA

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



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switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			'F11			SN54F11		SN74F11		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A, B, or C	Y	2.2	3.8	5.6	1.7	7.5	2.2	6.6	ns
t _{PHL}			1.7	3.7	5.5	1.2	7.5	1.7	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

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SN74F11, Triple 3-input positive-AND gates

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54F11	SN74F11
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-1/20
No. of Gates	3	3
Static Current		7.95
tpd max (ns)		6.6

FEATURES

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- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

DESCRIPTION

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TECHNICAL DOCUMENTS

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DATASHEET

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Full datasheet in Acrobat PDF: [sn74f11.pdf](#) (67 KB, Rev.A) (Updated: 10/01/1993)

APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs \(Rev. A\)](#) (SCBA012A - Updated: 08/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)

RELATED DOCUMENTS

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View Related Documentation for [Digital Logic](#)

- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74F11D	ACTIVE	SOP (D) 14	0 TO 70	View Contents	1KU 0.24	50	N/A*	400 19 Sep	5 WKS	Avnet AMERICA	115	BUY NOW
								> 10k 07 Oct				
								> 10k 14 Oct				
								> 10k 21 Oct				
SN74F11DR	ACTIVE	SOP (D) 14	0 TO 70	View Contents	1KU 0.22	2500	709	5000 24 Sep	5 WKS	Avnet AMERICA	> 1k	BUY NOW
								6316 04 Oct				
								> 10k 11 Oct				
								> 10k 18 Oct				
SN74F11N	ACTIVE	PDIP (N) 14	0 TO 70	View Contents	1KU 0.22	25	850	9175 19 Sep	5 WKS	Avnet AMERICA	391	BUY NOW
								4 25 Sep				
								> 10k 04 Oct				
								> 10k 07 Oct				
SN74F11N3	OBSOLETE	PDIP (N) 14	0 TO 70	View Contents	1KU		N/A*		Not Available			
SN74F11NSR	ACTIVE	SOP (NS) 14		View Contents	1KU 0.24	2000	N/A*	152 23 Sep	5 WKS			
								4000 03 Oct				
								> 10k 07 Oct				

								> 10k 14 Oct				
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Table Data Updated on: 9/26/2002