National Semiconductor

MM54HC646/MM74HC646 Non-Inverting Octal Bus Transceiver/Registers
MM54HC648/MM74HC648 Inverting Octal Bus Transceiver/Registers

General Description

These transceivers utilize advanced silicon-gate CMOS technology, and contain two sets of TRI-STATE® outputs, two sets of D-type flip-flops, and control circuitry designed for high speed multiplexed transmission of data.

Six control inputs enable this device to be used as a latched transceiver, unlatched transceiver, or a combination of both. As a latched transceiver, data from one bus is stored for later retrieval by the other bus. Alternately real time bus data (unlatched) may be directly transferred from one bus to another.

Circuit operation is determined by the G, DIR, CAB, CBA, SAB, SBA control inputs. The enable input, G, controls whether any bus outputs are enabled. The direction control, DIR, determines which bus is enabled, and hence the direction data flows: The SAB, SBA inputs control whether the latched data (stored in D type flip flops), or the bus data (from other bus input pins) is transferred. Each set of flip-flops has its own clock CAB, and CBA, for storing data. Data is latched on the rising edge of the clock.

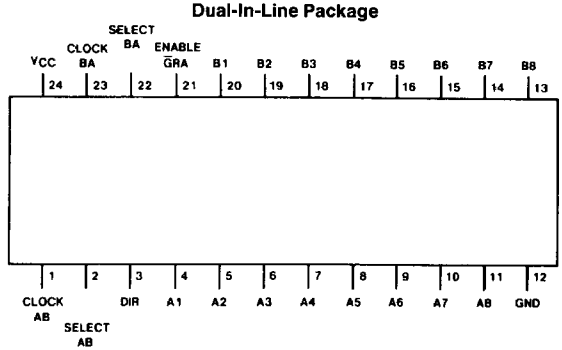
Each output can drive up to 15 low power Schottky TTL loads. These devices are functionally and pin compatible to their LS-TTL counterparts. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- TRI-STATE outputs
- Bidirectional communication
- Wide power supply range: 2–6V
- Low quiescent supply current: 160 μA maximum (74HC)
- High output current: 6 mA (74HC)

Connection Diagram

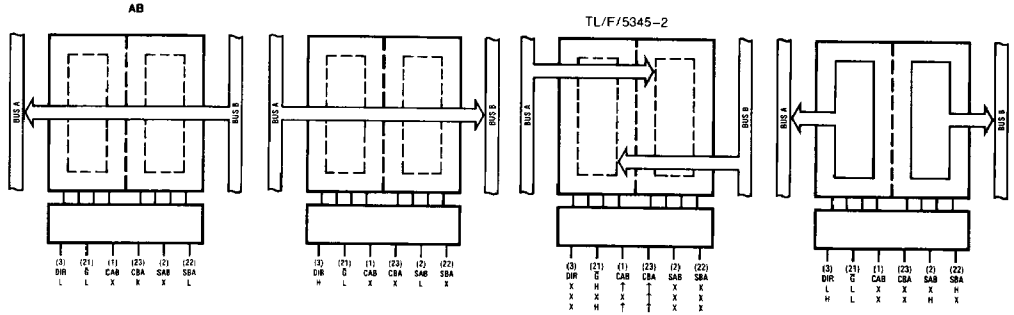
Dual-In-Line Package



Order Number MM54HC646/648* or MM74HC646/648*

*Please look into Section 8, Appendix D for availability of various package types.

TL/F/5345–2



Real-Time Transfer Bus B to Bus A | **Real-Time Transfer Bus A to Bus B** | **Storage from A, B, or A and B** | **Transfer Stored Data to A or B**

TL/F/5345–1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.96	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.46	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

Truth Table

Inputs						Data I/O		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
X	X	↑	X	X	X	Input	Not Specified	Store A, B Unspecified	Store A, B Unspecified
X	X	X	↑	X	X	Not Specified	Input	Store B, A Unspecified	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage

Truth Table (Continued)

Inputs						Data I/O		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

H = High Level L = Low Level X = Irrelevant ↑ = low-to-high level transition

The data output functions i.e., data at the bus pins may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled.

The data output functions i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

AC Electrical Characteristics MM54HC646/MM74HC646, MM54HC648/MM74HC648

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=45$ pF	14	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=45$ pF	31	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=45$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	$C_L=45$ pF	35	50	ns
t_{PZH}, t_{PZL}	Maximum Enable Time $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=45$ pF	18	33	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time, $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=5$ pF	17	30	ns

AC Electrical Characteristics MM54HC646/MM74HC646, MM54HC648/MM74HC648

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=50$ pF	2.0V	60	180	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	18	26	31	39	ns
		$C_L=150$ pF	6.0V	22	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=50$ pF	2.0V	110	220	275	330	ns
		$C_L=150$ pF	2.0V	150	270	338	405	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	40	54	68	81	ns
		$C_L=50$ pF	6.0V	28	38	47	57	ns
		$C_L=150$ pF	6.0V	34	47	59	71	ns

AC Electrical Characteristics MM54HC646/MM74HC646, MM54HC648/MM74HC648 (Continued)

V_{CC} = 2.0 − 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output	C_L = 50 pF	2.0V	85	170	214	253	ns
		C_L = 150 pF	2.0V	110	220	277	328	ns
		C_L = 50 pF	4.5V	17	34	43	51	ns
		C_L = 150 pF	4.5V	22	44	55	66	ns
		C_L = 50 pF	6.0V	14	29	36	43	ns
		C_L = 150 pF	6.0V	19	37	47	56	ns
t_{PZL}, t_{PZL}	Maximum Output Enable Time, $\overline{G}$ Input or DIR to A or B Output	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	80	175	219	263	ns
		C_L = 150 pF	2.0V	120	225	281	338	ns
		C_L = 50 pF	4.5V	23	35	44	53	ns
		C_L = 150 pF	4.5V	31	45	56	68	ns
		C_L = 50 pF	6.0V	21	30	37	45	ns
		C_L = 150 pF	6.0V	27	38	48	57	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, $\overline{G}$ Input to A or B Output	R_L = 1 kΩ	2.0V	85	175	219	263	ns
		C_L = 50 pF	4.5V	23	35	44	53	ns
			6.0V	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Clock		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram