

HI-307/883

T-51-11

Dual SPDT CMOS Analog Switch

January 1989

Features

- This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Analog Signal Range ($\pm 15V$ Supplies)..... $\pm 15V$
- Low Leakage ($+25^{\circ}C$)..... $1nA$ (Max)
- Low Leakage ($+125^{\circ}C$)..... $100nA$ (Max)
- Low ON Resistance..... 50Ω (Max)
- Charge Injection..... $30pC$ (Typ)
- CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power
- Compatible with DG307

Applications

- Sample and Hold, i.e. Low Leakage Switching
- Op Amp Gain Switching, i.e. Low ON Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

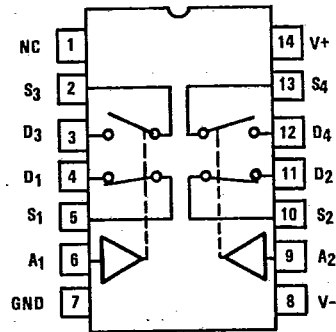
The HI-307/883 switch is a monolithic device fabricated using CMOS technology and the Harris Dielectric Isolation process. This switch features break-before-make switching, low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

The HI-307/883 is CMOS compatible and has a logic "0" condition with an input less than 3.5V and a logic "1" condition with an input greater than 11V.

The HI-307/883 is pin-for-pin compatible with the industry standard Siliconix DG307. The device is available in a 14 pin Ceramic DIP. The HI-307/883 operates over the $-55^{\circ}C$ to $+125^{\circ}C$ temperature range.

Pinout

HI-307/883 (CERAMIC DIP)
TOP VIEW



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

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Specifications HI-307/883

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Absolute Maximum Ratings

Voltage Between V+ and V- Terminals	44V
$\pm V_{SUPPLY}$ to Ground (V+, V-)	$\pm 22V$
Analog Input Voltage +V _S	+V _{SUPPLY} +1.5V
-V _S	-V _{SUPPLY} -1.5V
Digital Input Voltage +V _A	+V _{SUPPLY} +4V
-V _A	-V _{SUPPLY} -4V
Peak Current (S or D) (Pulse at 1ms, 10% Duty Cycle Max)	40mA
Continuous Current	30mA
Junction Temperature	+175°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	$\leq 275^\circ C$

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
-Ceramic DIP Package	88°C/W	24°C/W
Package Power Dissipation at +75°C		
-Ceramic DIP Package	0.85W	
Package Power Dissipation Derating Factor Above +75°C		
-Ceramic DIP Package	11.36mW/°C	

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range	-55°C to +125°C	Logic Low Level (V _{AL})	0V to 3.5V
Operating Supply Voltage ($\pm V_{SUPPLY}$)	$\pm 15V$	Logic High Level (V _{AH})	11V to +V _{SUPPLY}
Analog Input Voltage (V _S)	$\pm V_{SUPPLY}$		

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, GND = 0V, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Switch "ON" Resistance	R _{DS}	V _{A1} = 11V, V _D = 10V, I _S = -10mA V _{A2} = 3.5V S1/S2/S3/S4	1	+25°C	-	50	Ω
			2,3	-55°C to +125°C	-	75	Ω
		V _{A1} = 11V, V _D = -10V, I _S = 10mA V _{A2} = 3.5V S1/S2/S3/S4	1	+25°C	-	50	Ω
			2,3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	I _{S(OFF)}	V _S = +14V, V _D = -14V, V _{A1} = 3.5V V _{A2} = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2,3	-55°C to +125°C	-100	100	nA
		V _S = -14V, V _D = +14V, V _{A1} = 3.5V V _{A2} = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2,3	-55°C to +125°C	-100	100	nA
Drain "OFF" Leakage Current	I _{D(OFF)}	V _S = -14V, V _D = +14V, V _{A1} = 3.5V V _{A2} = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2,3	-55°C to +125°C	-100	100	nA
		V _S = +14V, V _D = -14V, V _{A1} = 3.5V V _{A2} = 11V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2,3	-55°C to +125°C	-100	100	nA
Channel "ON" Leakage Current	I _{D(ON)}	V _D = V _S = +14V, V _{A1} = 11V V _{A2} = 3.5V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2,3	-55°C to +125°C	-100	100	nA
		V _D = V _S = -14V, V _{A1} = 11V V _{A2} = 3.5V S1/S2/S3/S4	1	+25°C	-1	1	nA
			2,3	-55°C to +125°C	-100	100	nA
Low Level Input Current	I _{AL}	All Channels V _{AL} = 3.5V	1	+25°C	-1.0	1.0	μA
			2,3	-55°C to +125°C	-1.0	1.0	μA
High Level Input Current	I _{AH}	All Channels V _{AH} = 11V	1	+25°C	-1.0	1.0	μA
			2,3	-55°C to +125°C	-1.0	1.0	μA
Supply Current	+I _{CC}	All Channels V _A = 0V	1	+25°C	-	10	μA
			2,3	-55°C to +125°C	-	100	μA
		All Channels V _A = 15V	1	+25°C	-	10	μA
			2,3	-55°C to +125°C	-	100	μA
Supply Current	-I _{CC}	All Channels V _A = 0V	1	+25°C	-10	-	μA
			2,3	-55°C to +125°C	-100	-	μA
		All Channels V _A = 15V	1	+25°C	-10	-	μA
			2,3	-55°C to +125°C	-100	-	μA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: +VSUPPLY = +15V, -VSUPPLY = -15V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn "ON" Time	t(ON)	CL = 33pF RL = 300Ω	9	+25°C	-	250	ns
			10, 11	-55°C, +125°C	-	500	ns
Turn "OFF" Time	t(OFF)	CL = 33pF RL = 300Ω	9	+25°C	-	150	ns
			10, 11	-55°C, +125°C	-	450	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: +VSUPPLY = +15V, -VSUPPLY = -15V, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Switch Input Capacitance	CIS(OFF)	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	CC1	VA = 0V	1	+25°C	-	10	pF
	CC2	VA = 15V	1	+25°C	-	10	pF
Switch Output Capacitance	COS	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	VISO	f = 1MHz, VGEN = 1Vp-p	1	+25°C	40	-	dB
Crosstalk	VCT	f = 1MHz, VGEN = 1Vp-p	1	+25°C	40	-	dB
Charge Transfer	VCTE	VS = GND, CL = 0.01μF	1	+25°C	-	15	mV

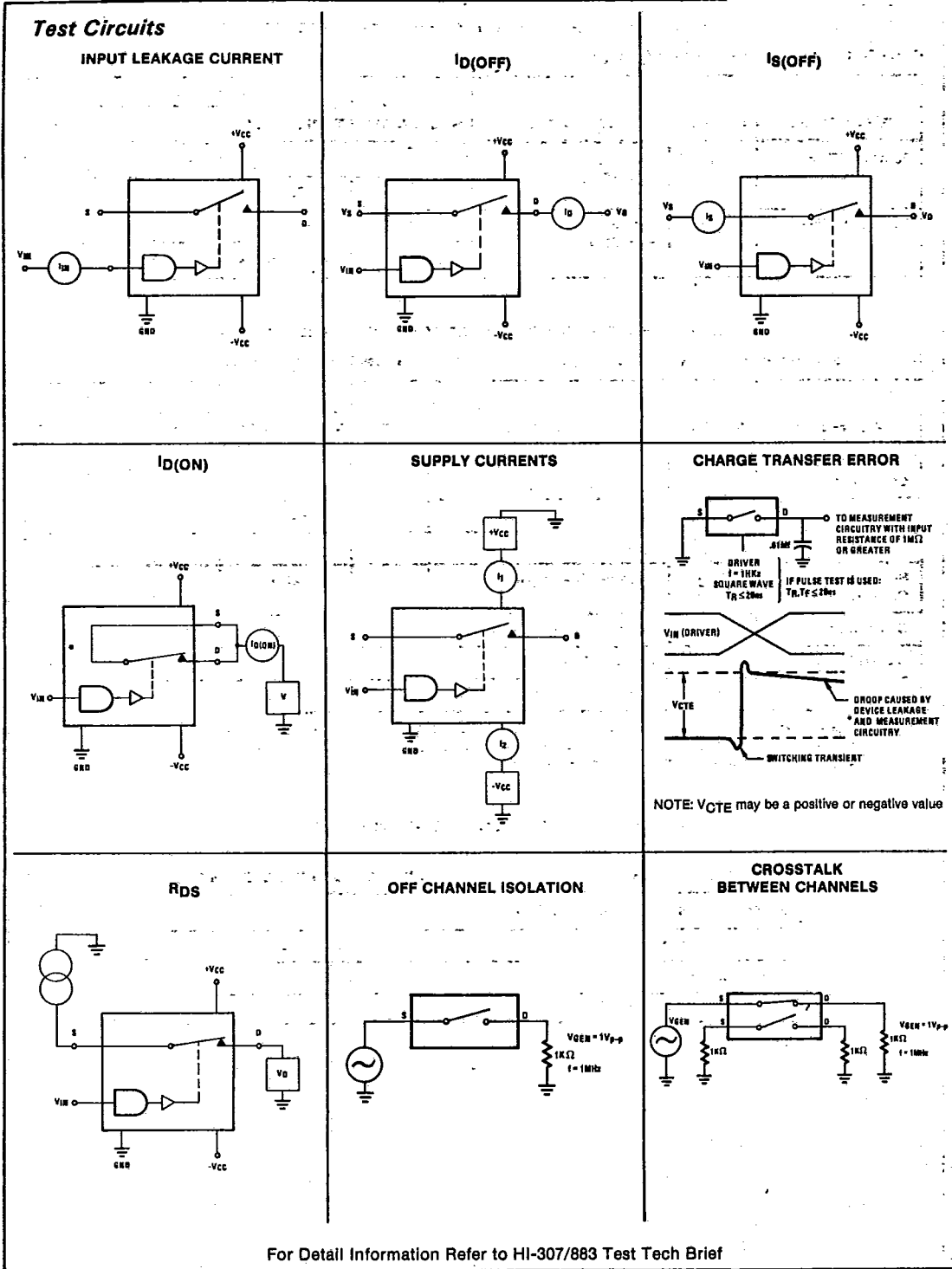
NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

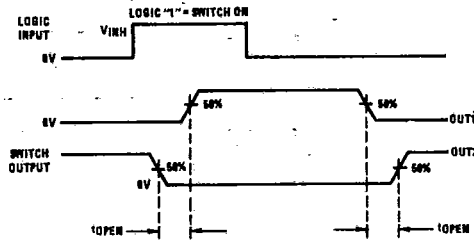
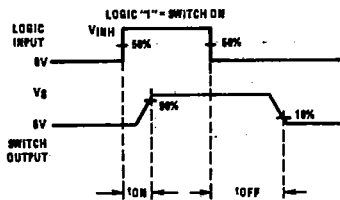
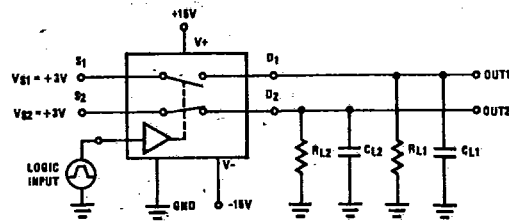
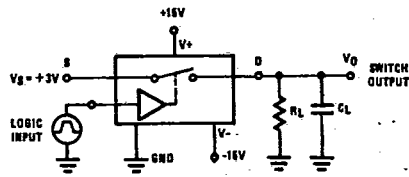
* PDA applies to Subgroup 1 only.

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For Detail Information Refer to HI-307/883 Test Tech Brief

Test Waveforms



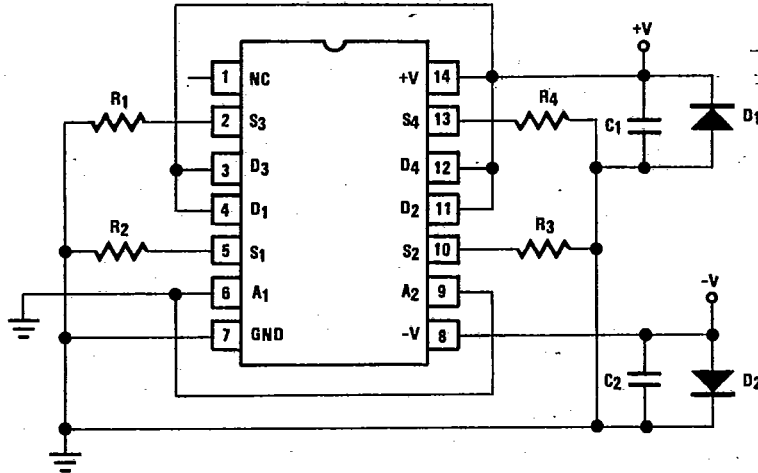
NOTES:

1. $R_L = R_{L1} = R_{L2} = 300\Omega$; $C_L = C_{L1} = C_{L2} = 33pF$
2. $V_{INH} = 15V$
 RISETIME (1.5V to 13.5V) $\leq 20ns$
 FALLTIME (13.5V to 1.5V) $\leq 20ns$

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Burn-In Circuit

HI-307/883 CERAMIC DIP

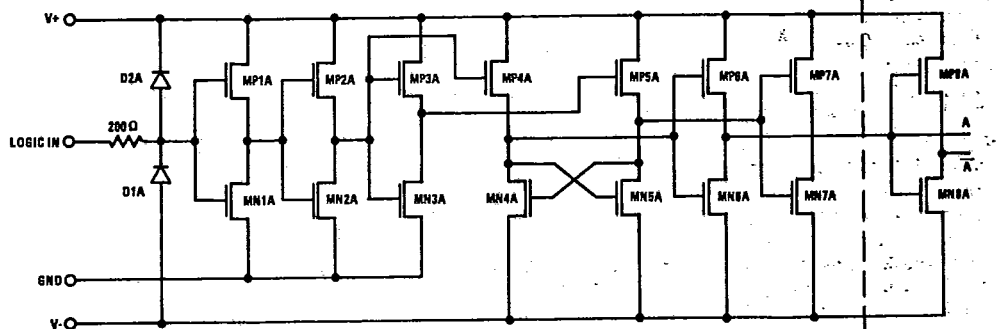


NOTES:

- R₁ = R₂ = R₃ = R₄ = 10KΩ, 5%, 1/4 or 1/2 watt
- C₁ = C₂ = 0.01μF (per socket) or 0.1μF (per row)
- D₁ = D₂ = 1N4002 (per board)
- |V₊ - V₋| = 30V

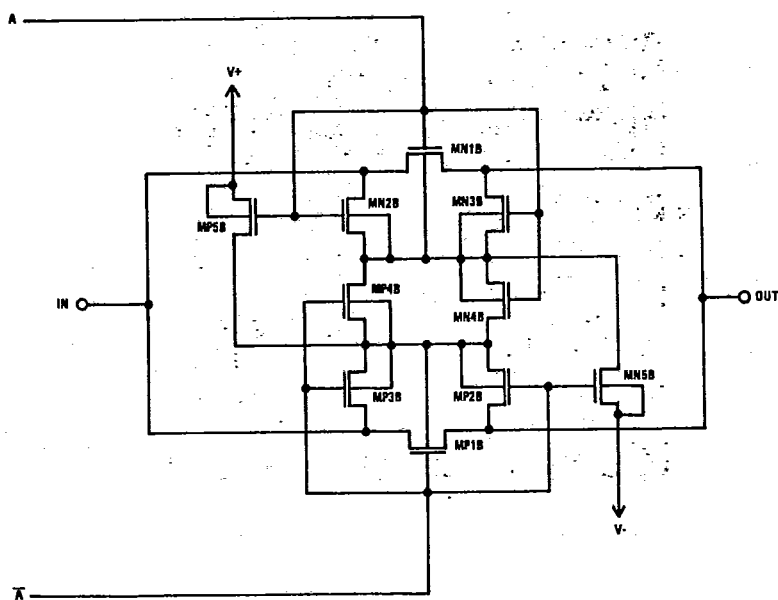
HARRIS SEMICONDUCTOR
Schematic Diagram

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL DRIVER
(ONE PER SWITCH CELL)

SWITCH CELL



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Die Characteristics

DIE DIMENSIONS:

76 x 83.9 x 19 mils

METALLIZATION:

Type: Aluminum
 Thickness: $16k\text{\AA} \pm 2k\text{\AA}$

GLASSIVATION:

Type: Nitride
 Thickness: $7k\text{\AA} \pm 0.7k\text{\AA}$

DIE ATTACH:

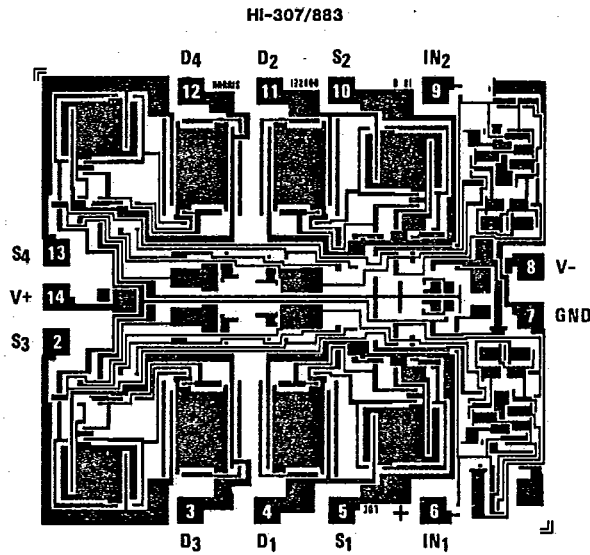
Material: Gold/Silicon Eutectic Alloy
 Temperature: Ceramic DIP — 460°C (Max)

WORST CASE CURRENT DENSITY:

$3.9 \times 10^5 \text{A/cm}^2$ at 30mA

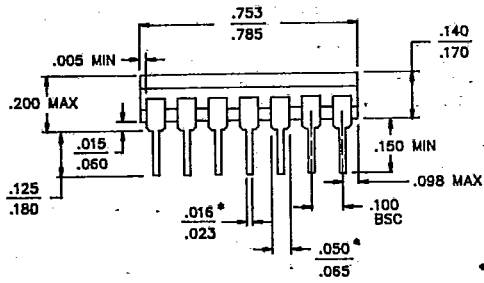
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

Metallization Mask Layout



Packaging†

14 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
 Material: Glass Frit
 Temperature: 450°C ± 10°C
 Method: Furnace Seal

INTERNAL LEAD WIRE:
 Material: Aluminum
 Diameter: 1.25 Mil
 Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

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NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†MIL-M-38510 Compliant Materials, Finishes, and Dimensions.



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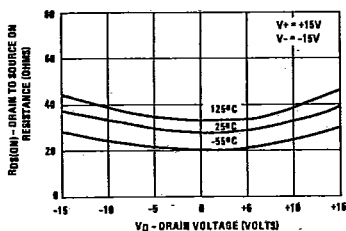
DESIGN INFORMATION

Dual SPDT CMOS Analog Switch

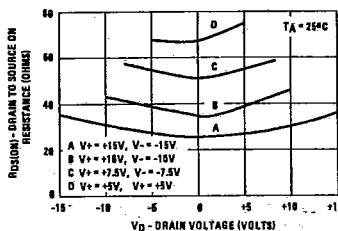
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: $V_+ = +15V$, $V_- = -15V$, $T_A = +25^\circ C$

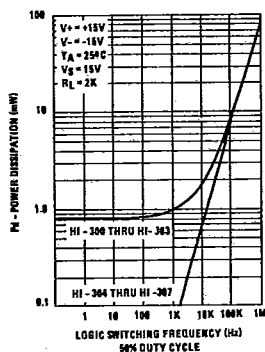
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



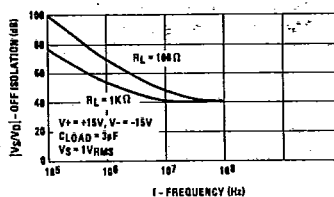
$R_{DS(ON)}$ vs. V_D AND POWER SUPPLY VOLTAGE



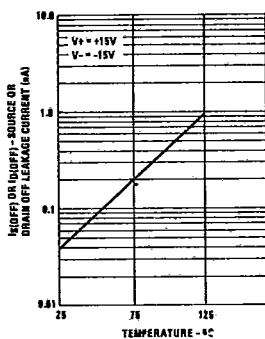
DEVICE POWER DISSIPATION vs. SWITCHING FREQUENCY SIGNAL LOGIC INPUT



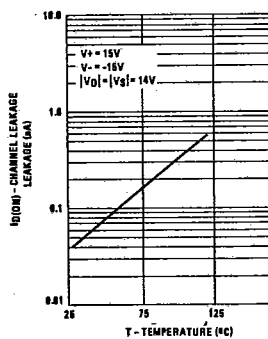
OFF ISOLATION vs. FREQUENCY



$I_S(OFF)$ or $I_D(OFF)$ vs. TEMPERATURE*



$I_D(ON)$ vs. TEMPERATURE*



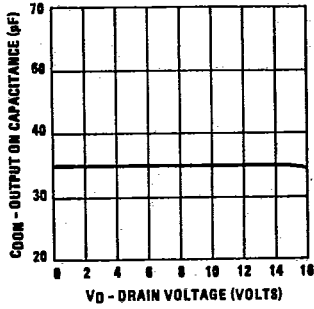
* The net leakage into the source or drain is the N-channel leakage minus the P-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

DESIGN INFORMATION (Continued)

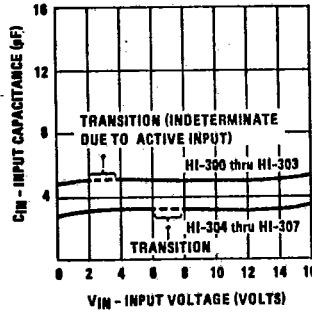
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Typical Performance Characteristics Unless Otherwise Specified: $V^+ = +15V$, $V^- = -15V$, $T_A = +25^\circ C$

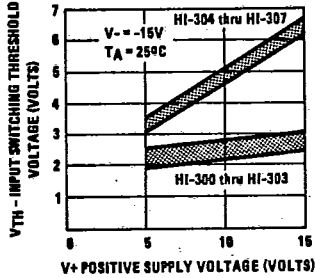
OUTPUT ON CAPACITANCE vs. DRAIN VOLTAGE



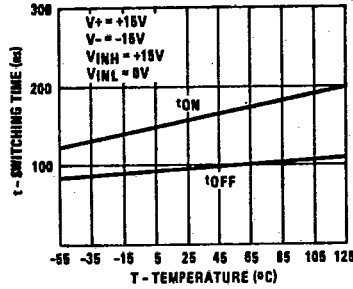
DIGITAL INPUT CAPACITANCE vs. INPUT VOLTAGE



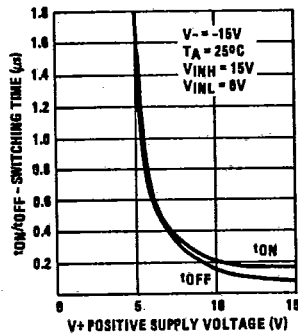
INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



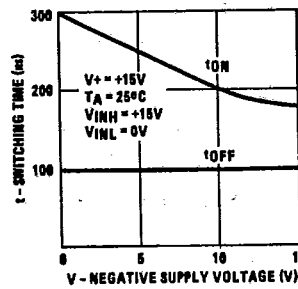
SWITCHING TIME vs. TEMPERATURE



SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



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