



# ICS85314I-01

LOW SKEW, 1-TO-5

DIFFERENTIAL-TO-2.5V/3.3V LVPECL FANOUT BUFFER

## GENERAL DESCRIPTION

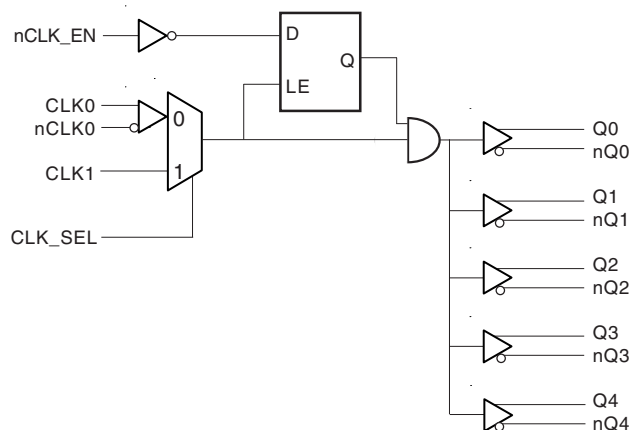
The ICS85314I-01 is a low skew, high performance 1-to-5 Differential-to-2.5V/3.3V LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS85314I-01 has two selectable clock inputs. The CLK0, nCLK0 pair can accept most standard differential input levels. The single-ended CLK1 can accept LVCMOS or LVTTTL input levels. The clock enable is internally synchronized to eliminate runt clock pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS85314I-01 ideal for those applications demanding well defined performance and repeatability.

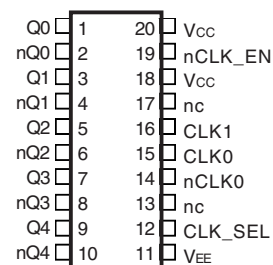
## FEATURES

- 5 differential 2.5V/3.3V LVPECL outputs
- Selectable differential CLK0, nCLK0 or LVCMOS inputs
- CLK0, nCLK0 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- CLK1 can accept the following input levels: LVCMOS or LVTTTL
- Maximum output frequency: 700MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 30ps (maximum), TSSOP package  
50ps (maximum), SOIC package
- Part-to-part skew: 350ps (maximum)
- Propagation delay: 1.8ns (maximum)
- RMS phase jitter @ 155.52MHz (12kHz - 20MHz): 0.05ps (typical)
- LVPECL mode operating voltage supply range:  $V_{CC} = 2.375V$  to  $3.8V$ ,  $V_{EE} = 0V$
- $-40^{\circ}C$  to  $85^{\circ}C$  ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT



### ICS85314I-01 20-Lead TSSOP

6.5mm x 4.4mm x 0.92mm Package Body  
**G Package**  
Top View

### ICS85314I-01 20-Lead SOIC

7.5mm x 12.8mm x 2.3mm Package Body  
**M Package**  
Top View



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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
5, 6	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.
7, 8	Q3, nQ3	Output		Differential output pair. LVPECL interface levels.
9, 10	Q4, nQ4	Output		Differential output pair. LVPECL interface levels.
11	V <sub>EE</sub>	Power		Negative supply pin.
12	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0, nCLK0 inputs. LVTTTL / LVCMOS interface levels.
13, 17	nc	Unused		No connect.
14	nCLK0	Input	Pullup	Inverting differential clock input.
15	CLK0	Input	Pulldown	Non-inverting differential clock input.
16	CLK1	Input	Pulldown	Clock input. LVTTTL / LVCMOS interface levels.
18, 20	V <sub>CC</sub>	Power		Positive supply pins.
19	nCLK_EN	Input	Pulldown	Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Q outputs are forced low, nQ outputs are forced high. LVTTTL / LVCMOS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

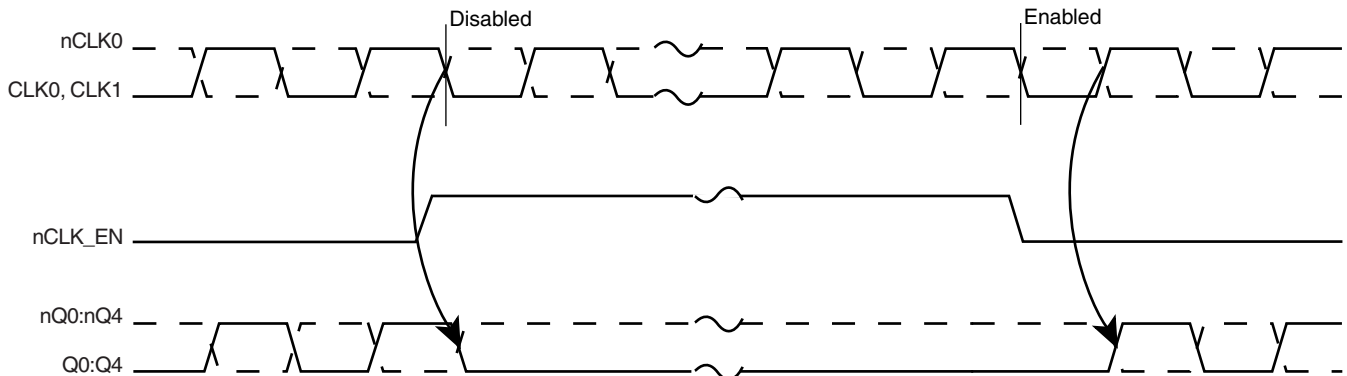


**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

Inputs			Outputs	
nCLK_EN	CLK_SEL	Selected Source	Q0:Q4	nQ0:nQ4
0	0	CLK0, nCLK0	Enabled	Enabled
0	1	CLK1	Enabled	Enabled
1	0	CLK0, nCLK0	Disabled; LOW	Disabled; HIGH
1	1	CLK1	Disabled; LOW	Disabled; HIGH

After nCLK\_EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK0, nCLK0 and CLK1 inputs as described in Table 3B.



**FIGURE 1. nCLK\_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

Inputs		Outputs		Input to Output Mode	Polarity
CLK0 or CLK1	nCLK0	Q0:Q4	nQ0:nQ4		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting



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### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_i$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_o$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	
20 Lead TSSOP	73.2°C/W (0 lfpm)
20 Lead SOIC	46.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 2.375V$  TO  $3.8V$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		2.375	3.3	3.8	V
$I_{EE}$	Power Supply Current				80	mA

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = 2.375V$  TO  $3.8V$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	nCLK_EN, CLK_SEL	2		$V_{CC} + 0.3$	V
		CLK1	2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	nCLK_EN, CLK_SEL	-0.3		0.8	V
		CLK1	-0.3		1.3	V
$I_{IH}$	Input High Current	CLK1, CLK_SEL, nCLK_EN $V_{IN} = V_{CC} = 3.8V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK1, CLK_SEL, nCLK_EN $V_{CC} = 3.8V, V_{IN} = 0V$	-5			$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = 2.375V$  TO  $3.8V$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	nCLK0 $V_{CC} = V_{IN} = 3.8V$			5	$\mu A$
		CLK0 $V_{CC} = V_{IN} = 3.8V$			150	$\mu A$
$I_{IL}$	Input Low Current	nCLK0 $V_{CC} = 3.8V, V_{IN} = 0V$	-150			$\mu A$
		CLK0 $V_{CC} = 3.8V, V_{IN} = 0V$	-5			$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		0.5		$V_{CC} - 0.85$	V

NOTE 1: For single ended applications the maximum input voltage for CLK0, nCLK0 is  $V_{CC} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .



**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = 2.375V$  TO  $3.8V$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 5. AC CHARACTERISTICS,  $V_{CC} = 2.375V$  TO  $3.8V$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{MAX}$	Output Frequency	CLK0, nCLK0			700	MHz	
		CLK1			300	MHz	
tjit ( $\emptyset$ )	RMS Phase Jitter (Random); NOTE 5	Integration Range: (12kHz - 20MHz)		0.05		ps	
$t_{pLH}$	Propagation Delay, Low to High; NOTE 1		1.0	1.4	1.8	ns	
tsk(o)	Output Skew; NOTE 3, 6	TSSOP Package			30	ps	
		SOIC Package			50	ps	
tsk(pp)	Part-to-Part Skew; NOTE 4, 6				350	ps	
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps	
odc	Output Duty Cycle	CLK0, nCLK0	$f \leq 700MHz$	45		55	%
		CLK1	$f \leq 250MHz$	45		55	%

All parameters measured at  $f_{MAX}$  unless noted otherwise.

The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Measured from  $V_{CC}/2$  input crossing point to the differential output crossing point.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 5: Please refer to the Phase Noise Plot.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

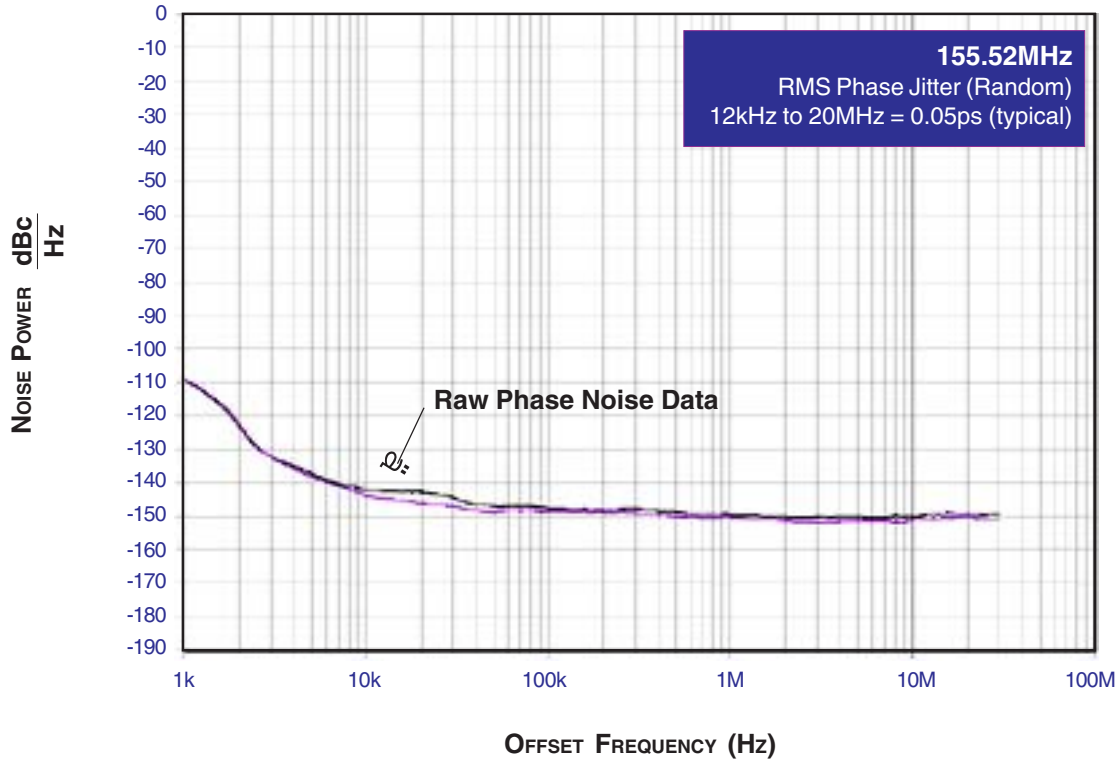


**ICS85314I-01**

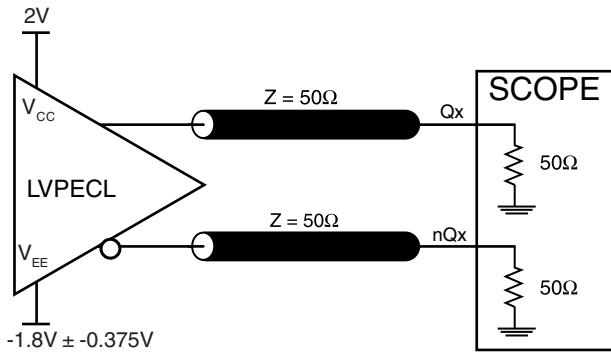
LOW SKEW, 1-TO-5

DIFFERENTIAL-TO-2.5V/3.3V LVPECL FANOUT BUFFER

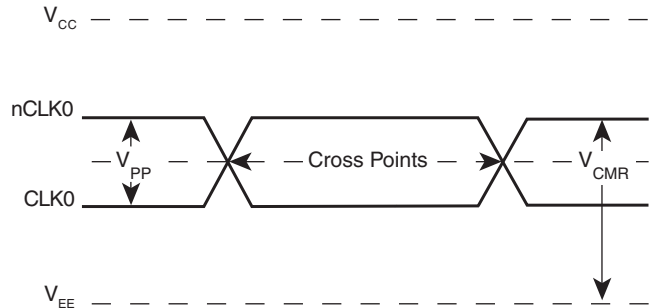
**TYPICAL PHASE NOISE AT 155.52MHz**



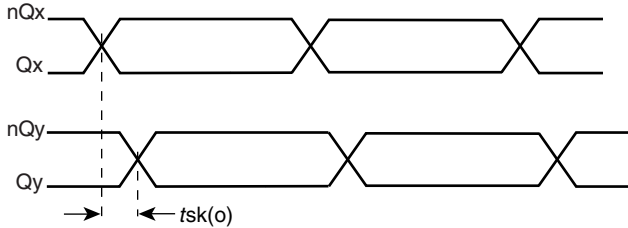
## PARAMETER MEASUREMENT INFORMATION



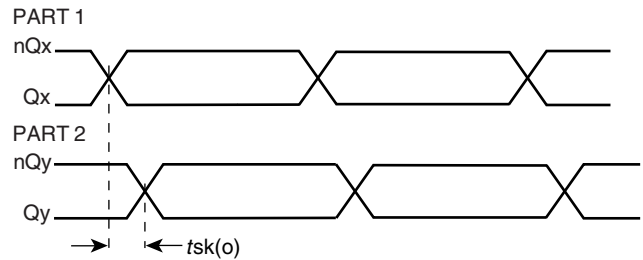
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



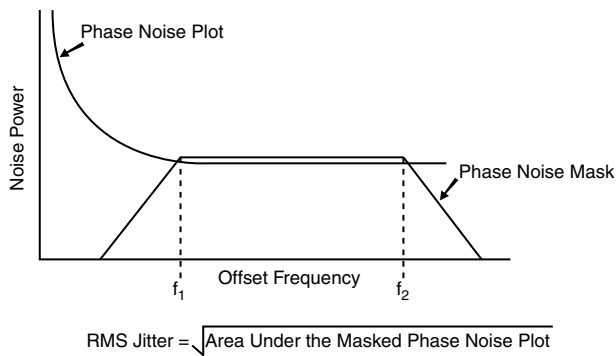
**DIFFERENTIAL INPUT LEVEL**



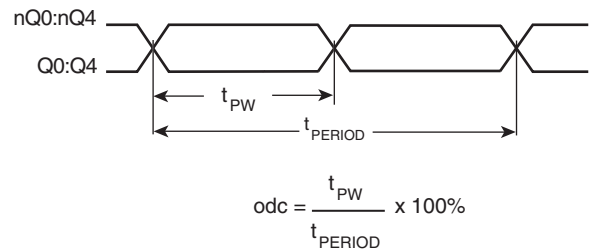
**OUTPUT SKEW**



**PART-TO-PART SKEW**



**RMS PHASE JITTER**



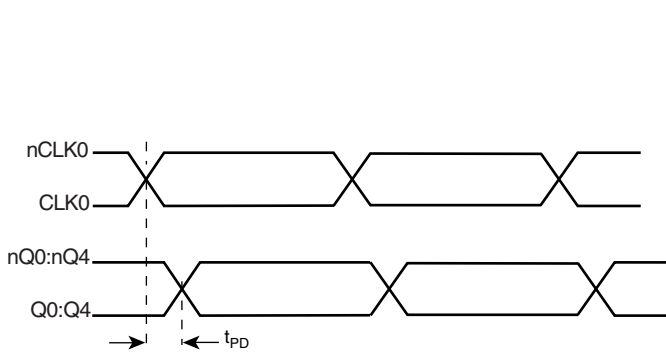
**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



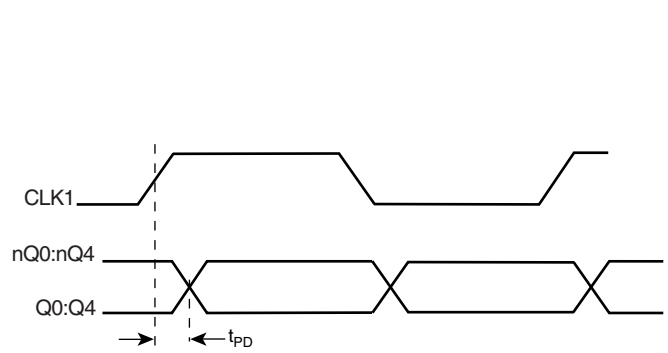
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LOW SKEW, 1-TO-5

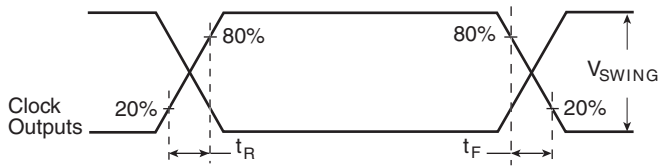
DIFFERENTIAL-TO-2.5V/3.3V LVPECL FANOUT BUFFER



PROPAGATION DELAY (DIFFERENTIAL INPUT)



PROPAGATION DELAY (LVCMOS INPUT)



OUTPUT RISE/FALL TIME



## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

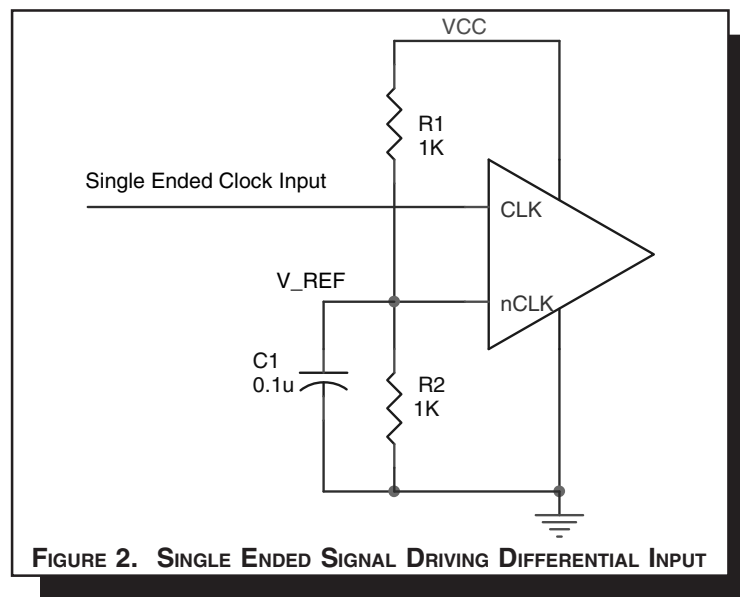


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CLK INPUT:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the CLK input to ground.

##### CLK/nCLK INPUT:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from CLK to ground.

##### LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### OUTPUTS:

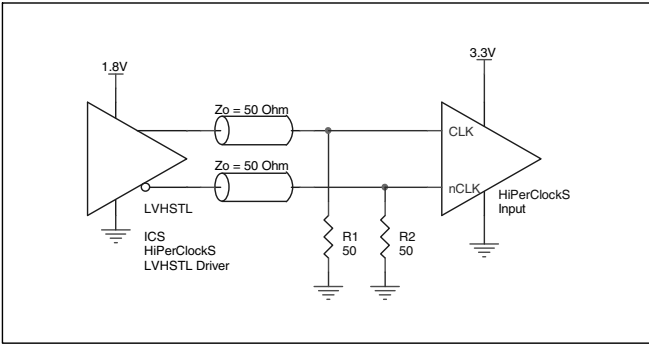
##### LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

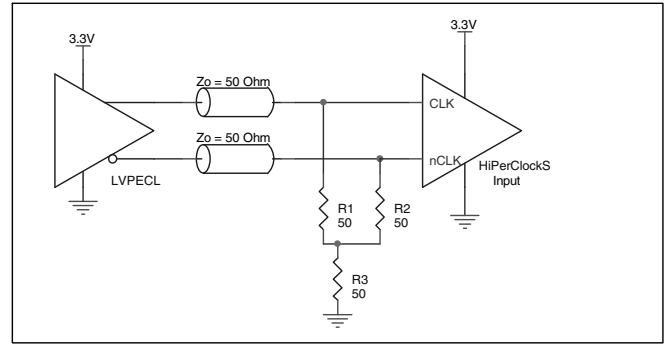
#### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

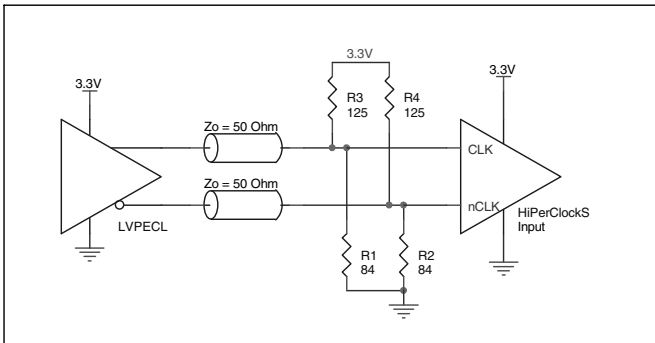
here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



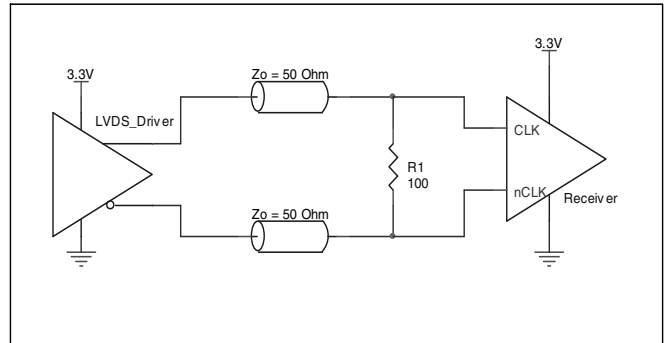
**FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



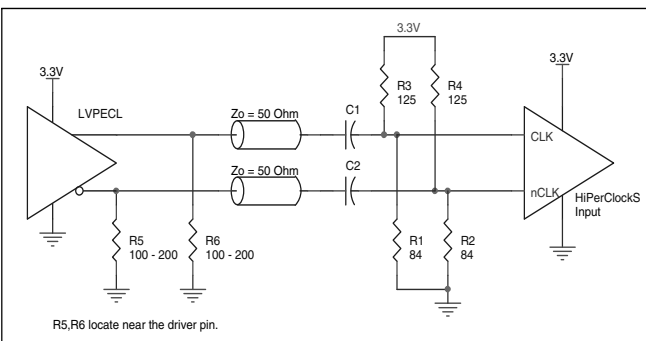
**FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



**FIGURE 3E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**

#### TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

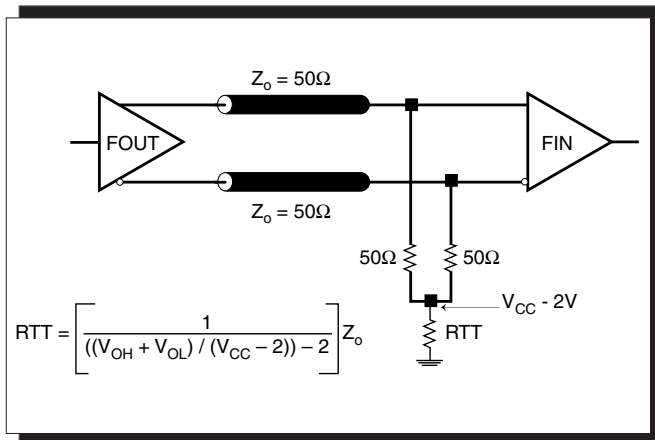


FIGURE 4A. LVPECL OUTPUT TERMINATION

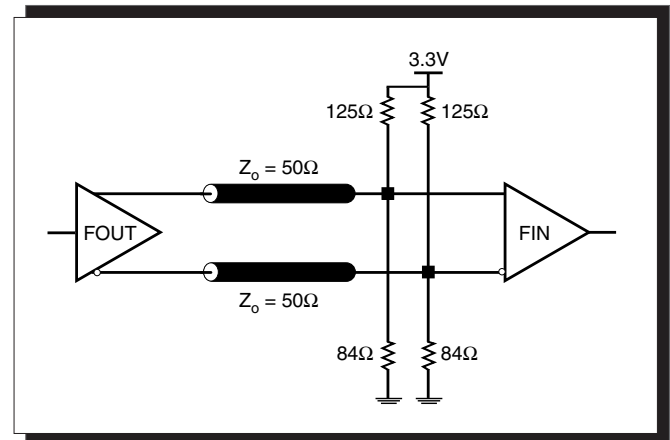


FIGURE 4B. LVPECL OUTPUT TERMINATION

#### TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very

close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

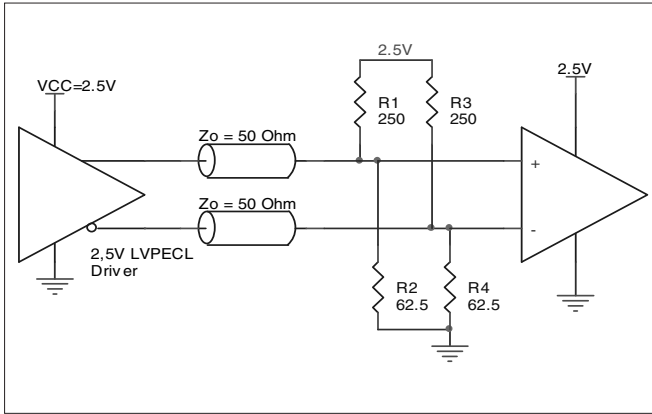


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

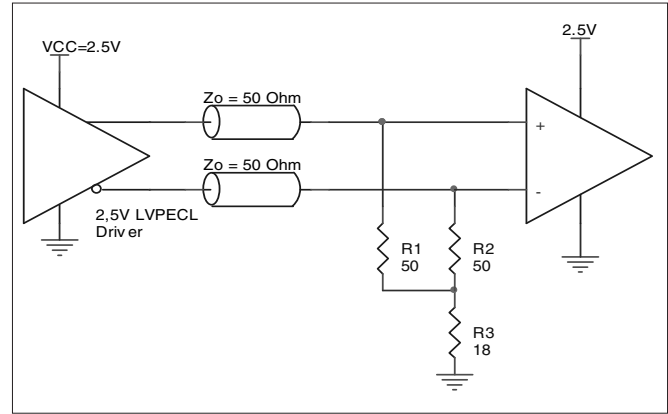


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

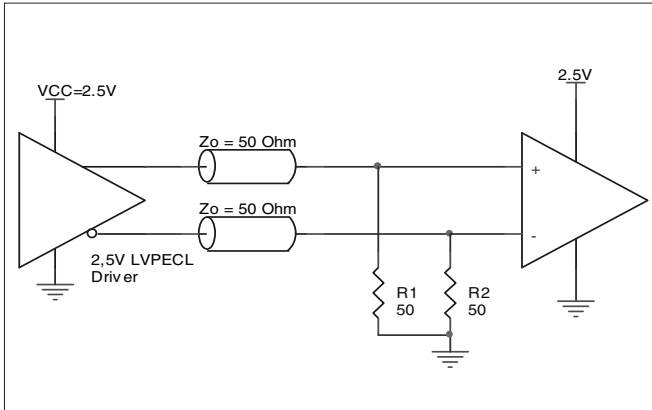


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85314I-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS85314I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.8V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.8V * 80mA = 304mW$
- Power (outputs)<sub>MAX</sub> = **30.2mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $5 * 30.2mW = 151mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $304mW + 151mW = 455mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6A below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85°C + 0.455W * 66.6°C/W = 115°C$ . This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6A. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-PIN TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

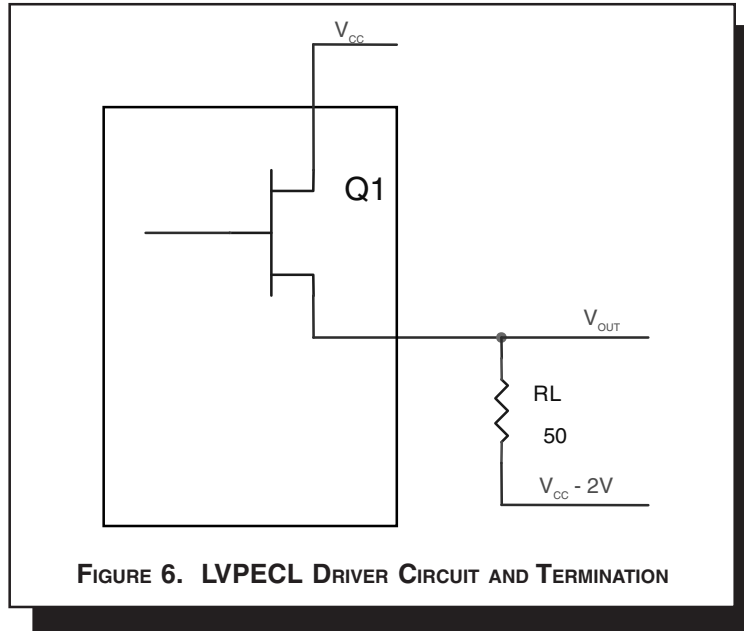
**TABLE 6B. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-PIN SOIC, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### 3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 6*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 1.0V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 1.0V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 1V)/50\Omega] * 1V = \mathbf{20.0mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = \mathbf{30.2mW}$



## RELIABILITY INFORMATION

**TABLE 7A.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 20 LEAD TSSOP**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**TABLE 7B.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 20 LEAD SOIC**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS85314I-01 is: 674

Compatible to part number MC100LVEL14

#### PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

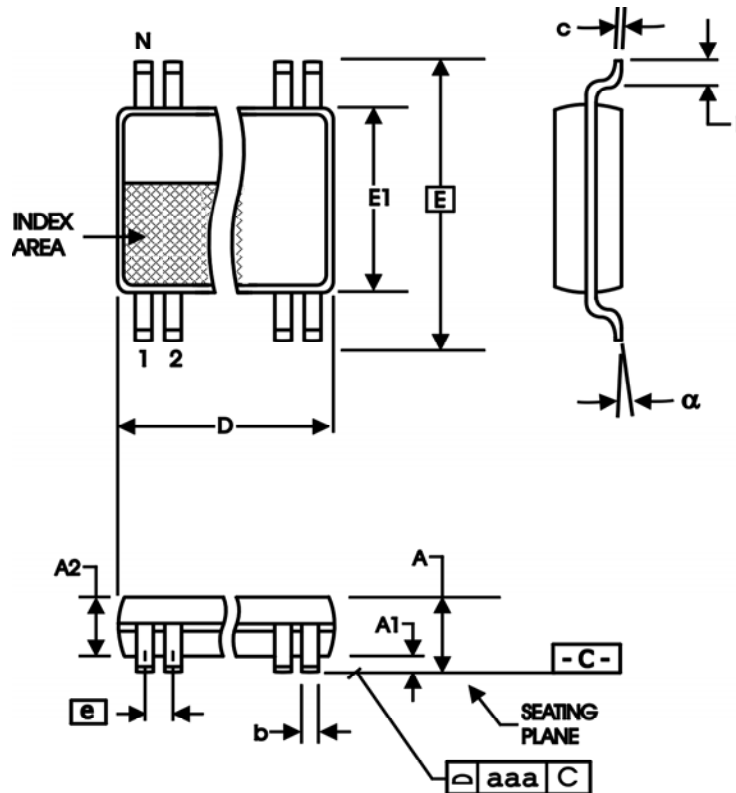


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
alpha	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



PACKAGE OUTLINE - M SUFFIX FOR 20 LEAD SOIC

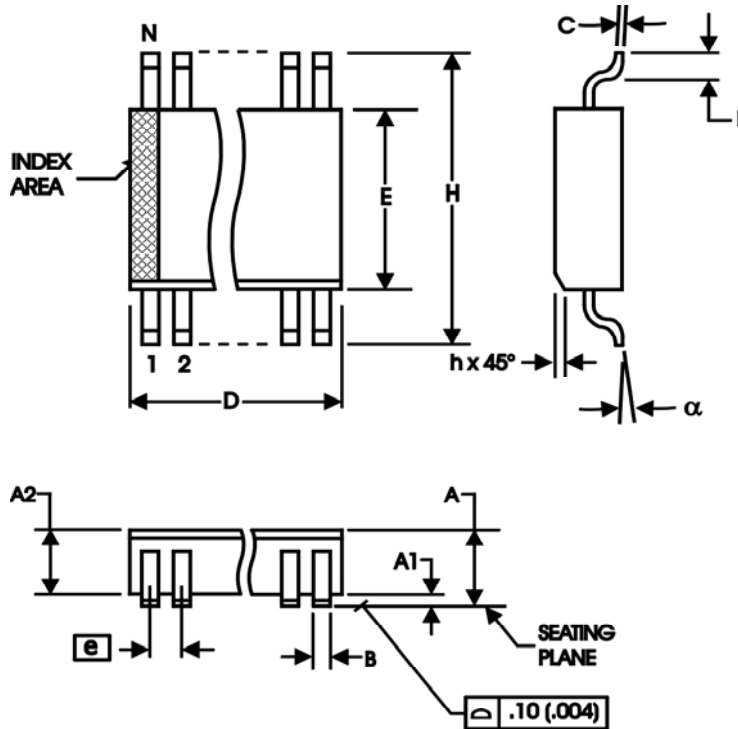


TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
$\alpha$	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119



# ICS85314I-01

LOW SKEW, 1-TO-5  
DIFFERENTIAL-TO-2.5V/3.3V LVPECL FANOUT BUFFER

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85314BGI-01	ICS85314BI01	20 lead TSSOP	tube	-40°C to 85°C
ICS85314BGI-01T	ICS85314BI01	20 lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS85314BGI-01LF	ICS5314BI01L	20 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS85314BGI-01LFT	ICS5314BI01L	20 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C
ICS85314BMI-01	ICS85314BI-01	20 lead SOIC	tube	-40°C to 85°C
ICS85314BMI-01T	ICS85314BI-01	20 lead SOIC	1000 tape & reel	-40°C to 85°C
ICS85314BMI-01LF	ICS85314BMI-01LF	20 lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS85314BMI-01LFT	ICS85314BMI-01LF	20 lead "Lead-Free" SOIC	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A		7	Updated Figure 2, Single Ended Signal Diagram.	3/31/03
		8	Added "Termination for 2.5V LVPECL Outputs" section.	
		9	Added "Differential Input Interface" section.	
		15	Corrected Order Number and Marking from Rev. A to Rev. B.	
B	T2 T5	1	Added Phase Noise Bullet to Features section.	8/11/04
		2	Changed $C_{IN}$ from 4pF max. to 4pF typical.	
		5	AC Characteristics Table - added RMS Phase Jitter.	
		6	Added Phase Jitter Plot.	
		8	Updated Termination for 3.3V LVPECL Output diagrams.	
		9	Updated Termination for 2.5V LVPECL Output section.	
C	T5	1	Features section - added SOIC package output skew.	3/22/05
		4	Absolute Maximum Ratings - added SOIC Package Thermal Impedance.	
		5	AC Characteristics table - added SOIC package for Output Skew.	
		7	Parameter Measurement Information - added Part-to-Part Skew and RMS Phase Jitter Diagrams.	
D	T5	1	Features section - changed Part-to-Part Skew from 250ps max. to 350ps max.	5/24/05
		5	AC Characteristics table - changed Part-to-Part Skew from 250ps max. to 350ps max.	
E	T4D	5	LVPECL DC Characteristics Table - changed $V_{OH}$ max from $V_{CC} - 1.0V$ to $V_{CC} - 0.9V$ .	9/23/05
		9	Application Information Section - added <i>Recommendations for Unused Input and Output Pins</i> .	
	T9	18	Added TSSOP Lead-Free part number.	
E	T9	18	Ordering Information Table - Added Lead Free marking	8/1/07