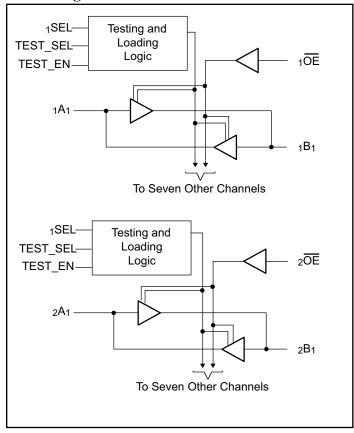


1.5V to 3.3V Universal Bi-directional Level Shifter with Automatic Direction Control & Advanced Package Solution

Features

- Designed for low voltage operation: 1.4V to 3.6V
- Universal bidirectional level shifting with automatic direction control
- Fast bus speeds up to 160 Mbps
- IOFF supports partial Power-Down mode operation
- Drive Capability 12mA
- · Independent translation of each bit
- · Each supply rail is configurable over supply range
- ESD Protection exceeds JESD22
 - 2000V Human Body Model (A114-B)
 - 200V Machine Model (A115-A)
- Latch-up performance exceeds 100mA per JESD 78
- Industrial operation at -40°C to +85°C
- Packaging (Pb-free & Green):
 - 45 lead TFBGA (NL)

Block Diagram



Description

Pericom Semiconductor's PI4ULS3V16M is a 16-bit (dual-octal) non-inverting bus transceiver with two separate supply rails. A port (V_{CCA}) and B port (V_{CCB}) are set to operate at 1.4V to 3.6V. This arrangement permits universal bidirectional translation of differential signal levels over the voltage ranges.

PI4ULS3V16M is designed for asynchronous communication between data buses. Data is transmitted from the A bus to the B bus, or vice versa, without direction control. All A_X , and B_X are tri-stated when data is coming from both directions at the same time. The output-enable (\overline{OE}) input is used to disable outputs so buses are isolated.

The control pins, SEL, TEST_EN and TEST_SEL are supplied by $V_{\rm CCB}$.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power-up or power-down, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Applications

- Voltage Translation
- · Bus Relay
- Mobile Terminals



Pin Configuration

1 2 3 4 5

A	TEST_EN	(1SEL)	TEST_SEL	$\overline{\left(1^{\overline{\mathrm{OE}}}\right)}$	(1^{A_1})
В	(1B ₁)	(V_{CC}^B)		$\left(V_{CC}^{A}\right)$	(1^{A_2})
C	(1B ₃)	$(1B_2)$		GND	GND
D	(1B5)	$\left(1^{\text{B}_4}\right)$		$\left(1^{A_3}\right)$	$\left(1^{A_4}\right)$
E	(1 ^B 7)	(1^{B_6})		(1^{A_6})	(1^{A_5})
F	$2B_1$	$(1B_8)$		(1^{A_8})	(1^{A7})
G	2B ₃	(2^{B_2})		(2^{A_1})	(2^{A_2})
Н	$2B_5$	2^{B_4}		2^{A_4}	(2^{A_3})
J	2B7	$2B_6$		(2^{A_6})	$(2A_5)$
K	2B ₈	GND		(2^{A_8})	$(2A_7)$
L	GND	$\left(V_{CCB}\right)$		$\left(V_{CC}^{A}\right)$	$2\overline{OE}$

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Maximum Ratings

(Absolute maximum ratings over operating free-air temperature range, unless otherwise noted)

Supply voltage range:	V _{CCA} 0.5V to 4.6V	Input clamp current, I _{IK} (V _I <0)50mA		
(1)	V _{CCB} 0.5V to 4.6V	Output clamp current, I_{OK} (V_O <0)50mA		
	Control Inputs –0.5V to 4.6V	Continuous output current, IO±20mA		
Voltage Range applied to a or Power-Off state, V _{IO} ⁽¹⁾	ny I/O pins in the high-impedance:	Continuous current through V _{CCA} , V _{CCB} or GND±100mA		
	A Port	Package thermal impedance, $0_{JA}^{(3)}$:		
	B Port0.5V to 4.6V	A package 82°C/W		
Voltage Range applied to a	ny I/O pins in the High or Low	ZF package33°C/W		
state $V_{IO}^{(1, 2)}$:	A Port0.5V to V _{CCA} +0.5V B Port0.5V to V _{CCB} +0.5V	Storage temperature range, T _{STG} –65°C to 150°C		

Note:

- 1. The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 2. This value is limited to 3.6V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.
- 4. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Pin Description

Pin Name	Description
$_{X}\overline{OE}$	3-State Output Enable Inputs (Active LOW)
XSEL	Outputs Loading Selection
$\chi A\chi$	Side A Inputs/Outputs
$_{\rm X} {\rm B}_{\rm X}$	Side B Inputs/Outputs
TEST_EN	Enable Test Mode
TEST_SEL	Test Mode Selection
GND	Ground
$V_{\text{CCA}}, V_{\text{CCB}}$	Power

Truth Table⁽¹⁾

Inputs		Outputs Loading ⁽²⁾	Operation				
$x\overline{OE}$	1SEL	Outputs Loading V	Operation				
L	L	$31 pF \le C_L \le 50 pF$	Bus B data to Bus A,				
L	Н	$21pF \le C_L \le 30pF$	or Bus A data to Bus B				
Н	X		Z (Isolation)				

Notes:

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- 1. H = HIGH Signal Level
 - L = LOW Signal Level
 - X = Don't Care or Irrelevant
 - Z = High Impedence
- 2. Refer to Figure 1 for Output Loading Chart

Test Mode

TEST_EN	TEST_SEL	Condition				
L	X	Normal Operation				
Н	L	TEST MODE $A \rightarrow B$				
Н	Н	TEST MODE $B \rightarrow A$				

Automatic Direction Control & Advanced Package Solution



Recommended Operating Conditions(1, 2, 3)

Parameter	Des	cription	V _{CCI}	Min.	Max.	Units	
V _{CCA} , V _{CCB}	Supply Voltage			1.1	3.6		
			1.1V to 1.95V	0.65 x V _{CCI}			
$ m V_{IH}$	High-Level Input Voltage	I/O pins	2.3V to 2.7V	1.7			
	voltage		2.7V to 3.6V	2			
			1.1V to 1.95V		0.35 x V _{CCI}		
$ m V_{IL}$	Low-Level Input Voltage	I/O pins	2.3V to 2.7V		0.7		
	voltage		2.7V to 3.6V		0.8		
			1.1V to 1.95V	0.65 x V _{CCB}			
$ m V_{IHB}$	High-Level Input Voltage	Control Inputs (OE and SEL)	2.3V to 2.7V	1.7		V	
	voltage	(OE and SEL)	2.7V to 3.6V	2			
	Low-Level Input Voltage		1.1V to 1.95V		0.35 x V _{CCB}		
$ m V_{ILB}$		Control Inputs (OE and SEL)	2.3V to 2.7V		0.7		
	Voltage	(OE and SEL)	2.7V to 3.6V		0.8		
V _I	Input Voltage	I/O pins and Control Inputs		0	3.6		
Vo	Output Voltage	I/O pins and Control Inputs		0	3.6		
			$V_{CCO} = 1.1V$		-3		
			$V_{CCO} = 1.4V$		-5		
I_{OH}	High-Level Output Current	I/O pins	$V_{CCO} = 1.65V$		-8		
	Current		$V_{CCO} = 2.3V$		-9		
			$V_{CCO} = 3.0V$		-12	†	
			$V_{CCO} = 1.1V$		3	mA	
			$V_{CCO} = 1.4V$		5		
$I_{ m OL}$	Low-Level Output Current	I/O pins	$V_{CCO} = 1.65V$		8	<u> </u>	
	Current		$V_{CCO} = 2.3V$		9		
			$V_{CCO} = 3.0V$		12		
Δt/ΔV	Input Transition rise	or fall rate			10	V/ns	
$T_{\mathbf{A}}$	Operating Free-Air	Temperature		-40	85	°C	

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Notes:

- 1. V_{CCI} is the V_{CC} associated with the data input port.
- 2. V_{CO} is the V_{CC} associated with the date output port.
- 3. To ensure proper device operation, all unused device inputs must be held at V_{CCI} or GND.



Electrical Characteristics for (Over recommended free-air temperature range, unless otherwise noted.)⁽⁷⁾

Parameter	Description	Test Conditions	V _{CCA} /V _{CCB}	Min.	Typ. (1)	Max.	Units	
		$I_{OH} = -100 \mu A$	1.1V to 3.6V	V _{CCO} - 0.1V				
		$I_{OH} = -2mA$	1.1V	0.8				
37	H' 1 I 10 4 4 1/14	$I_{OH} = -4mA$	1.4V	1				
V_{OH}	High-Level Output Voltage	$I_{OH} = -7mA$	1.65V	1.2				
		$I_{OH} = -9mA$	2.3V	1.8				
		$I_{OH} = -12mA$	3.0V	2.4			V	
		$I_{OL} = 100 \mu A$	1.1V to 3.6V			0.2	·	
		$I_{OL} = 2mA$	1.1V			0.3		
Vox	Low-Level Output Voltage	$I_{OL} = 4mA$	1.4V			0.4		
V_{OL}	Low-Level Output voltage	$I_{OL} = 7mA$	1.65V			0.4		
		$I_{OL} = 9mA$	2.3V			0.4		
		$I_{OL} = 12mA$	3.0V			0.4	0.4	
I_{CC}	Quiescent Supply Current	$V_I = V_{CCI}$ or GND, $I_O = 0$	1.1V to 3.6V			10		
I_{I}	Control Inputs (OE and SEL)	$V_I = V_{CCB}$ or GND	1.1V to 3.6V			±5	μΑ	
$I_{OZ}^{(6)}$	3-State Output Current	$V_O = V_{CCO}$ or GND	1.1V to 3.6V			±10		
I_{OFF}	Power-off Leakage Current	$V_{\rm I}$ or $V_{\rm O} = 0$ to 3.6V	0V			±10		
C_{IN}	Control Input Capacitance	$V_I = V_{CCB}$ or GND			3		nE	
C_{IO}	I/O Capacitance	$V_O = V_{CCA/B}$ or GND			5		pF	

Notes:

- 1. All typical values are at $T_A = 25$ °C.
- 2. The High-level minimum sustaining current that the bus-hold circuit can source at V_{IH} min. I_{BHH} is measured after raising V_{IN} to V_{CCA} and then lowering it to V_{IH} min.
- 3. The Low-level minimum sustaining current that the bus-hold circuit can sink at V_{IL} max. I_{BHL} is measured after lowering V_{IN} to GND and then raising it to V_{IL} Max.

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- 4. An external driver must sink as least I_{BHLO} to switch this node from High to Low.
- 5. An external driver must source at least I_{BHHO} to switch this node from Low to High.
- 6. For I/O ports, the parrameter I_{OZ} includes the input leakage current.
- 7. Parameters are specified under test mode conditions.



Timing Characteristics for $V_{CCA} = 1.5V \pm 0.1V$

(Over recommended free-air temperature range, unless otherwise noted.)

Parameter	From (Input) ($V_{\text{CCB}} = 1.5V$ $\pm 0.1V$		$V_{\text{CCB}} = 1.8V$ $\pm 0.15V$		$V_{\text{CCB}} = 2.5V$ $\pm 0.2V$		$V_{\text{CCB}} = 3.3V$ $\pm 0.3V$		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
,	A	В	1.0	7.0	1.0	6.5	1.0	6.0	1.0	5.0	
t_{PD}	В	A	1.0	7.0	1.0	6.5	1.0	6.0	1.0	5.5	ma.
$t_{SK(a)}^{(1)}$		-		0.3		0.3		0.3		0.3	ns
$t_{SK(b)}^{(1)}$				0.25		0.25		0.25		0.25	
$f_{\text{max}}^{(2)}$	Maximum	Frequency	40		60		80		80		MHz

Timing Characteristics for $V_{CCA} = 1.8V \pm 0.15V$

(Over recommended free-air temperature range, unless otherwise noted.)

Parameter	From (Input) (C	To (Output)	$V_{\text{CCB}} = 1.5V$ $\pm 0.1V$		$V_{\text{CCB}} = 1.8V$ $\pm 0.15V$		$V_{\text{CCB}} = 2.5V$ $\pm 0.2V$		$V_{\text{CCB}} = 3.3V$ $\pm 0.3V$		Units
		(Output)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
_	A	В	1.0	7.0	0.5	6.0	0.5	5.5	0.5	5.0	
t _{PD}	В	A	1.0	6.0	0.5	6.0	0.5	5.5	0.5	5.0	
$t_{SK(a)}^{(1)}$				0.25		0.25		0.25		0.25	ns
$t_{SK(b)}^{(1)}$				0.2		0.2		0.2		0.2	
$f_{MAX}^{(2)}$	Maximum F	requency	40		60		80		80		MHz

Timing Characteristics for $V_{CCA} = 2.5V \pm 0.2V$

(Over recommended free-air temperature range, unless otherwise noted.)

Parameter	From (Input)	To	$V_{\text{CCB}} = 1.5V$ $\pm 0.1V$		$V_{\text{CCB}} = 1.8V$ $\pm 0.15V$		$V_{CCB} = 2.5V$ $\pm 0.2V$		$V_{\text{CCB}} = 3.3V$ $\pm 0.3V$		Units
		(Output)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
4	A	В	1.0	6.0	0.5	5.5	0.5	5.0	0.5	4.5	
t _{PD}	В	A	1.0	6.0	0.5	5.5	0.5	5.0	0.5	4.5	
$t_{SK(a)}^{(1)}$				0.25		0.25		0.25		0.25	ns
$t_{SK(b)}^{(1)}$				0.2		0.2		0.2		0.2	
$f_{max}^{(2)}$	Maximum F	requency	40		60		80		80		MHz

Notes:

1. This is the skew between any two outputs of the same package, and switching in the same direction. For t_{SK(a)}, Output 1 and Output 2 are any two outputs. For t_{SK(b)}, Output 1 and Output 2 are in the same bank. These parameters are warranted but not production tested.

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- 2. Refer to Truth Table for Frequency Selections.
- 3. This parameter is specified under test mode conditions.



Timing Characteristics for $V_{CCA} = 3.0V \pm 0.3V$

(Over recommended free-air temperature range, unless otherwise noted.)

Parameter	I I	To (Output)	1 ±0.1 V 1		$V_{\text{CCB}} = 1.8V$ $\pm 0.15V$		$V_{\text{CCB}} = 2.5V$ $\pm 0.2V$		$V_{\text{CCB}} = 3.3V$ $\pm 0.3V$		Units
		(Output)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
,	A	В	1.0	6.0	0.5	5.0	0.5	4.5	0.5	4.0	
$t_{ m PD}$	В	A	1.0	5.5	0.05	5.0	0.5	4.5	0.5	4.0	
$t_{SK(a)}^{(1)}$				0.25		0.25		0.25		0.25	ns
$t_{SK(b)}^{(1)}$				0.2		0.2		0.2		0.2	
$f_{\text{max}}^{(2)}$	Maximum F	requency	40		60		80		80		MHz

Notes:

- 1. This is the skew between any two outputs of the same package, and switching in the same direction. For t_{SK(a)}, Output 1 and Output 2 are any two outputs. For t_{SK(b)}, Output 1 and Output 2 are in the same bank. These parameters are warranted but not poroduction tested.
- 2. Refer to Truth Table for Frequency Selections.
- 3. This parameter is specified under test mode conditions.

Operating Characteristics (V_{CCA} and $V_{CCB} = 2.5V$, $T_A = 25$ °C)

Paramete	er		Test Conditions	Тур.	Units	
	Dawer Dissinction Conscitance A to D	Outputs Enabled		13		
Cpd ⁽¹⁾ (V _{CCA})	Power Dissipation Capacitance A to B	Outputs Disabled	$C_L = 0$	28	ъE	
	Dawer Dissinction Conscitance D to A	Outputs Enabled	f = 10 MHz	17	pF	
	Power Dissipation Capacitance B to A	Outputs Disabled		30		
	Dawer Dissinction Conscitance A to D	Outputs Enabled		17	pF	
Cpd (1)	Power Dissipation Capacitance A to B	Outputs Disabled	$C_L = 0$	32		
(V _{CCB})	Dawer Dissinction Conscitance D to A	Outputs Enabled	f = 10 MHz	13		
	Power Dissipation Capacitance B to A	Outputs Disabled		28		

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Notes:

1. This parameter is specified under test mode conditions.



Parameter Measurement Information

V _{CCA} /V _{CCB}	$C_{ m L}$	$R_{ m L}$		Test	S1	
1.1V ~ 1.6V	10pF	2kΩ		t _{PLH} /t _{PHL}	Open	
1.8V ±0.15V	20pF	1kΩ		t _{PLZ} /t _{PZL}	2X V _{CCO}	
$2.5V \pm 0.2V$	30pF	500Ω		$t_{\mathrm{PHZ}}/t_{\mathrm{PZH}}$	GND	
$3.3V \pm 0.3V$	50pF	500Ω	_			
From Output Under Test mode CL	T	9 GND	In	put	$\begin{array}{c c} & t_{W} & & \downarrow \\ \hline \\ V_{CCI}/2 & & \downarrow \\ \end{array} V_{CCI}/2 & 0V \\ \end{array}$	
Test Circuit for t_{DIS} / t_{EN}				Voltage Waveforms Enable and Disable Times		
Output				Enable and	Disable Times	
Output		1 Open			Disable Times	
OutputCL				Output		
			(lov	Output Control v-level	/VCCE	
CL	<u></u>) Open	(lov	Output Control v-level	VCCB/2 VCCB/2	
CL) Open	C (lov ena	Output Control v-level abling)	VCCB/2 VCCB/2 VCCB/2 VCCB/2 VCCB/2	
Test C	<u></u>) Open	C (lov ena C Wavefo S1 at 2x\	Output Control w-level abling) Output tpZL VCCO	VCCB/2 VCCB/2 VCCB/2 VCCB/2 VCCC	
CL	ircuit for t _{pd}	Open t _{sk}	C (lov ena O Wavefo	Output Control w-level abling) Output tpZL VCCO	VCCB/2 VCCB/2 VCCB/2 VCCO/2 VCCO/2 VCCO/2 VCCO/2	
Test C	ircuit for t _{pd}	o Open t _{sk} Vcc √cci/2	C (lov ena C Wavefo S1 at 2x\	Output Control w-level abling) Output trycco ote 2)	VCCB/2 VCCB/2 VCCB/2 VCCO/2	
Test C	ircuit for t _{pd}	Open t _{sk} Vcc Vccl/2 t _{PHL}	Cl (lov ena Cl Wavefo S1 at 2x\ (see no	Output Control w-level abling) Output orm 1 /CCO ote 2)	VCCB/2 VCCB/2 VCCB/2 VCCO/2 VCCO/2 VCCO/2 VOL+VA TPHZ VCCO	
Test Conput VCCI/2	ircuit for t _{pd}	Open t _{sk} VCCI/2 VHL TPHL VOI	C (lov ena	Output Control w-level abling) Output orm 1 VCCO ote 2) tpzH Output orm 2	VCCB/2 VCCB/2 VCCO/2	
Test Conput	ircuit for t _{pd}	Open t _{sk} Vcc Vccl/2 t _{PHL}	C (lov ena	Output Control v-level abling) Output orm 1 VCCO ote 2) tpzh tpzh dutput orm 2 GND	VCCB/2 VCCB/2 VCCB/2 VCCO/2 VCCO/2 VCCO/2 VOL+VA VCCO/2 VOL+VA	

Figure 1. Load Circuit and Voltage Waveforms

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Notes:

- 1. C_L includes probe and jig capacitance.
- 2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- 3. All input pulses are supplied by generators having the following characteristics: $PRR \le 10Mz$, $Z_O = 50\Omega$, $tr \le 2.5ns$, $tf \le 2.5ns$.
- 4. The outputs are measured one at a time with one transition per measurement.

Voltage Waveforms

Propagation Delay Times

- 5. t_{PLZ} and t_{PHZ} are the same as t_{DIS} .
- 6. t_{PZL} and t_{PZH} are the same as t_{EN} .
- 7. t_{PLH} and t_{PHL} are the same as t_{PD} .
- 8. V_{CCI} defines the input port (V_{CCA} or V_{CCB}).
- V_{CCO} defines the output port (V_{CCA} or V_{CCB}).

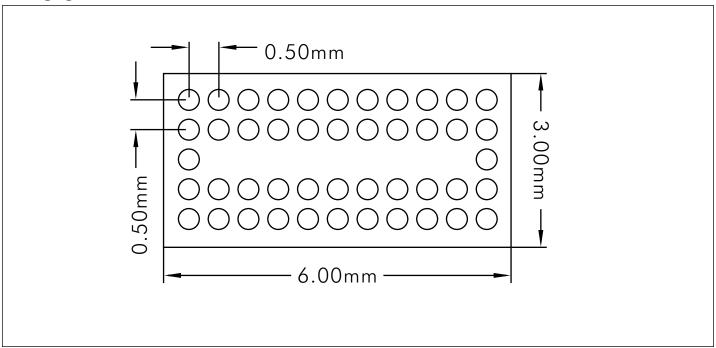
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Voltage Waveforms

Enable and Disable Times



Packaging Mechanical: 45-lead TBGA



Ordering Information

Ordering Code	Packaging Code	Package Description
PI4ULS3V16NLE	NL	Pb-free and Green 45-ball TFBGA

Notes:

- 1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- 2. Number of Transistors = TBD

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