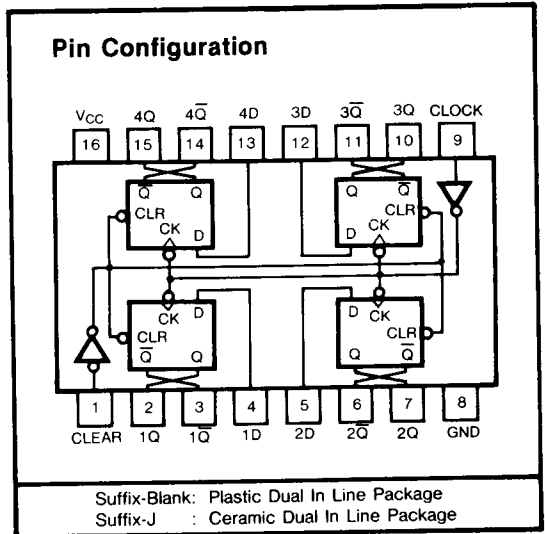# GD54/74LS175
QUAD D-TYPE FLIP-FLOPS

Feature

- Contains Four Flip-Flops with Double-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications: Buffer/Storage Registers
  Shift Registers
  Pattern Generators

Description

This monolithic, positive edge-triggered flip-flops utilize, TTL circuitry to implement D-type flip-flop logic.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.
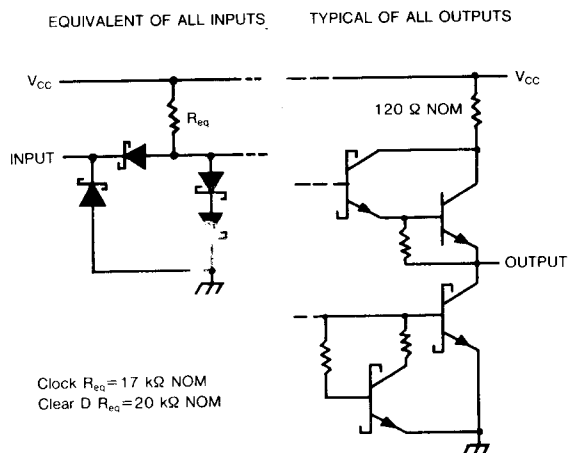
Pin Configuration

Suffix-Blank: Plastic Dual In Line Package
Suffix-J   : Ceramic Dual In Line Package

Function Table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑*	H	H	L
H	↑*	L	L	H
H	L	X	Q_0*	$\overline{Q}_0$

* ↑=transition from low to high level.
* Q_0 = the level of Q before the indicated steady-state input conditions were established.

Schematics of Inputs and Outputs

EQUIVALENT OF ALL INPUTS

TYPICAL OF ALL OUTPUTS

Clock R_{eq}=17 kΩ NOM
Clear D R_{eq}=20 kΩ NOM

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range   54LS .... −55°C to 125°C
  - 74LS .... 0°C to 70°C
- Storage temperature range .... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		30	MHz
t_w	Width of clock or clear pulse		20			ns
t_{su}	Set up time	Data input	20			ns
		Clear inactive-state	25			
t_h	Data hold time		5			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.7	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max	54	2.5	3.4		V
		I_{OH}=Max V_{IH}=Min	74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, (Note 3)			11	18	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
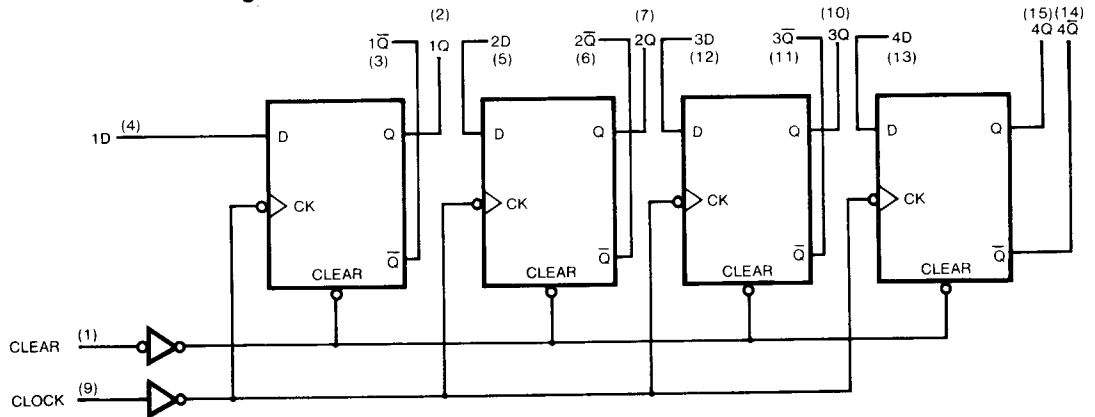Note 3: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics, $V_{CC} = 5V$, $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		30	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear	$C_L = 15pF$, $R_L = 2k\Omega$		20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			13	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			16	25	ns

For load circuit and voltage waveforms, see page 3-11.

Function Block Diagram

Application Example

TIMING PULSE GENERATOR