FAIRCHILD
SEMICONDUCTOR™

ML65T541

3.3V High Speed Octal Buffer/Line Driver

GENERAL DESCRIPTION

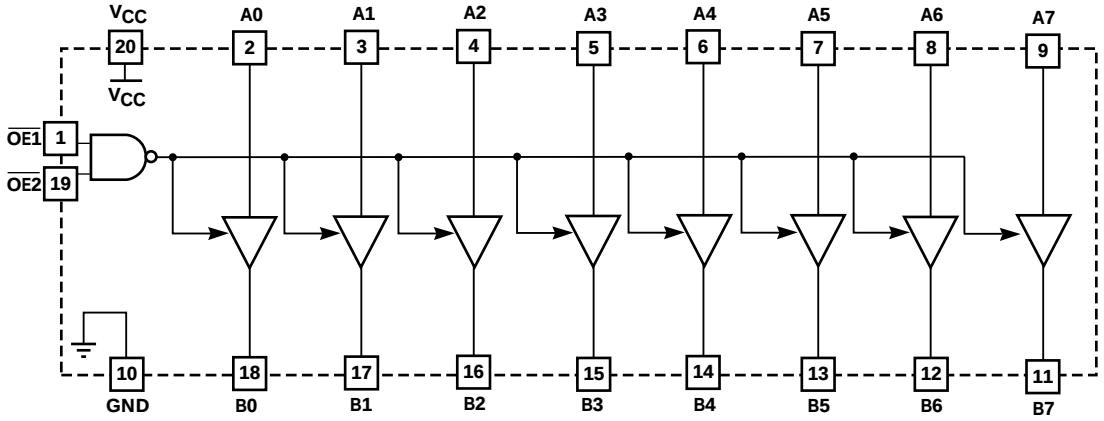
The ML65T541 is a non-inverting octal buffer/line driver. The high operating frequency (66MHz driving a 50pF load) and low propagation delay (2ns) make it ideal for very high speed applications such as processor bus buffering cache/main memory control.

The ML65T541 uses a unique analog implementation to eliminate the delays inherent in traditional digital designs. Schottky clamps reduce undershoot and overshoot, and special output driver circuits limit ground bounce. The ML65T541 conforms to the pinout and functionality of the industry standard FCT541 and is intended for applications where propagation delay is critical to the system design.

FEATURES

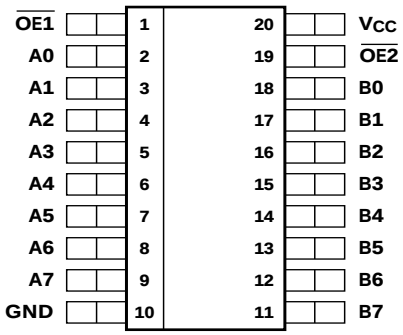
- Low propagation delay — 2.0ns
- Fast 8-bit buffer/line driver with three-state capability on the output
- Schottky diode clamps on all inputs to handle undershoot and overshoot
- Onboard schottky diodes minimize noise
- Ground bounce controlled outputs
- Industry standard FCT541 type pinout
- Applications include high speed cache memory, main memory, processor bus buffering, and graphics cards

BLOCK DIAGRAM



Pin Configuration

20-Pin SOIC, QSOP



TOP VIEW

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
Ai	I	Data Bus A
Bi	O	Data Bus B
$\overline{OE}1$ & $\overline{OE}2$	I	Output Enable
GND	I	Signal Ground
V_{CC}	I	3.3V supply

FUNCTION TABLE

$\overline{OE}1/\overline{OE}2$	A	B
H	X	Z
L	L	L
L	H	H

L = Logic Low
H = Logic High
X = Don't Care
Z = High Impedance

Absolute Maximum Ratings

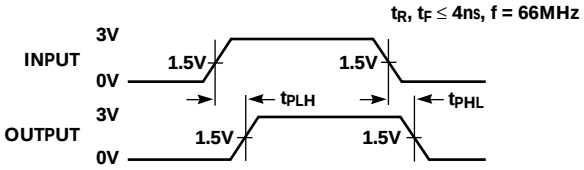
V_{CC} ..... –0.3V to 7V
DC Input voltage ..... –0.3 to V_{CC} + 0.3V
AC Input voltage (< 20ns) ..... –3.0V
DC Output voltage ..... –0.3 to V_{CC} + 0.3V
Output sink current (per pin) 120mA
Storage temperature ..... –65°C to 150°C
Junction temperature ..... 150°C
Thermal Impedance (θ_{JA})
SOIC ..... 96°C/W
QSOP ..... 100°C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for: V_{CC} = 3.3V ± 10%, T_A = 0°C to 70°C (Note 1)

symbol	parameter	conditions	min	typ	max	units
AC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} = 500ý)						
t_{PLH}, t_{PHL}	Propagation delay	Ai to Bi (Note 2)		1.4	2.0	ns
t_{OE}	Output enable time $\overline{OE}1$, $\overline{OE}2$ to Bi			10	20	ns
t_{OD}	Output disable time $\overline{OE}1$, $\overline{OE}2$ to Bi			15	20	ns
C_{IN}	Input capacitance			8		pF
DC ELECTRICAL CHARACTERISTICS (C_{LOAD} = 50pF, R_{LOAD} =)						
V_{IH}	Input high voltage	Logic HIGH (Note 3)	2.0			V
V_{IL}	Input low voltage	Logic LOW (Note 3)			0.8	V
I_{IH}	Input high current	Per pin, V_{IN} = 3V		0.2	0.8	mA
I_{IL}	Input low current	Per pin, V_{IN} = 0		0.3	0.8	mA
I_{HI-Z}	Three-state output current	$0 < V_{IN} < V_{CC}$			5	µA
I_{OS}	Short circuit current	V_O = GND (Note 4)	–60		–225	mA
V_{IC}	Input clamp voltage	I_{IN} = 18mA		–0.7	–1.2	V
V_{OH}	Output high voltage	I_{OH} = 100µA (Note 5)	2.4			V
V_{OL}	Output low voltage	I_{OL} = 5mA (Notes 5,6)			0.6	V
I_{CC}	Quiescent Power Supply Current	Freq = 0Hz, V_{IN} = 0V, outputs open		55	80	mA

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.
Note 2: One line switching, see Figure 3, t_{PLH}, t_{PHL} versus C_L.
Note 3: Inputs should be driven to within 0.3V of the rail. Although the inputs are TTL compatible, at the minimum logic high voltage, the circuit will draw current due to the buffer action (³ 20mA per channel).
Note 4: Not more than one output should be shorted for more than a second.
Note 5: See Figure 2 for I_{OH} versus V_{OH} and I_{OL} versus V_{OL} data.
Note 6: The output can source or sink more than 100 mA when switching. I_{OL} is only significant as a DC specification.



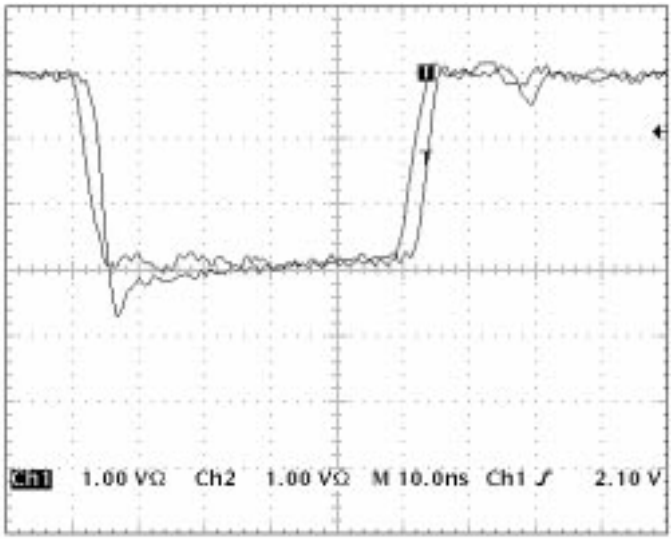


Figure 1. Typical Switching Waveform, Four Outputs Switching into 50pF Loads.

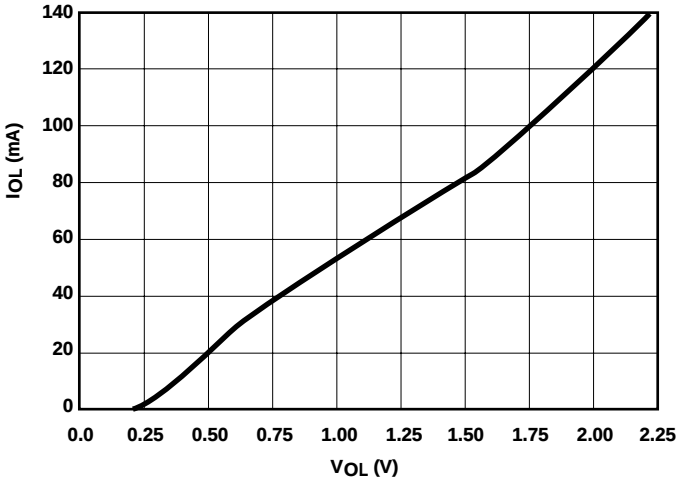


Figure 2a. Typical VOL Versus IOL for One Buffer Output.

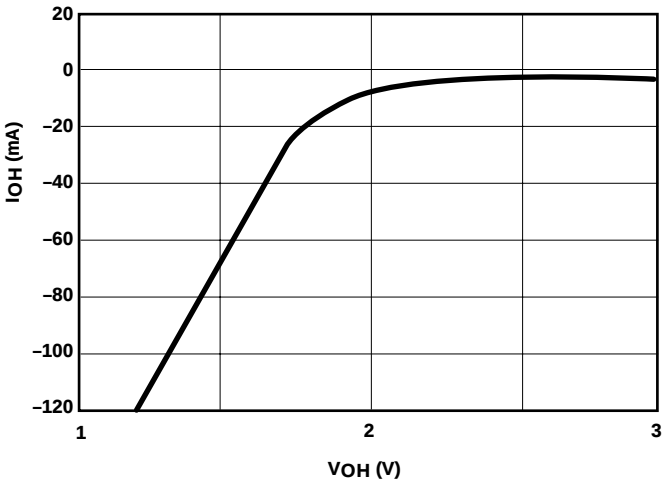


Figure 2b. Typical VOH Versus IOH for One Buffer Output.

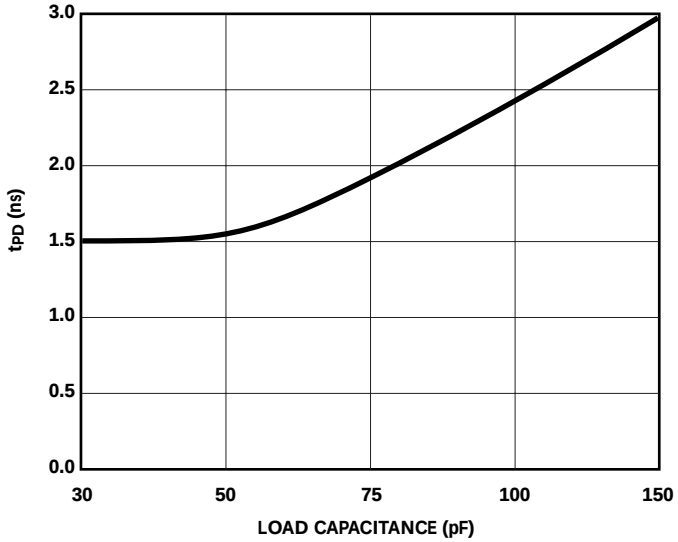


Figure 3. Propagation Delay (tPLH, tPHL) Versus Load Capacitance, One Output Switching At 66MHz.

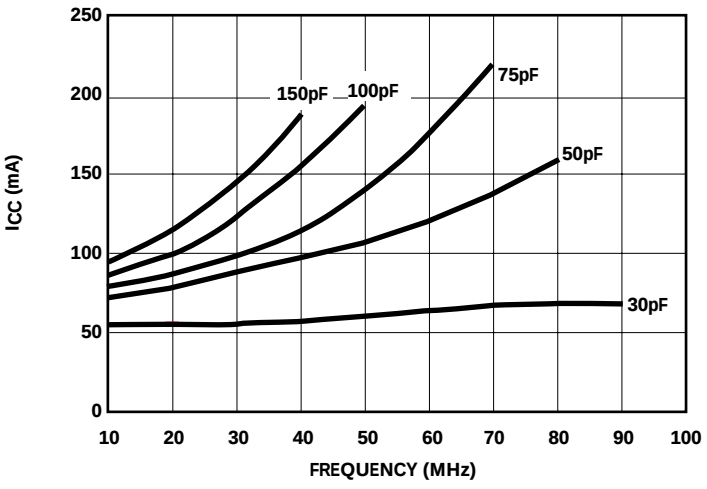


Figure 4. ICC Versus Frequency for Various Load Capacitances, Four Outputs Switching.

FUNCTIONAL DESCRIPTION

The ML65T541 is a very high speed non-inverting buffer/ line driver with three-state outputs which is ideally suited for bus-oriented applications. It provides a low propagation delay by using an analog design approach (a high speed unity gain buffer), as compared to conventional digital approaches. The ML65T541 follows the pinout and functionality of the industry standard FCT541 series of buffers/line drivers and is intended to replace them in designs where the propagation delay is a critical part of the system design considerations. The ML65T541 is capable of driving load capacitances several times larger than its input capacitance. It is configured so that the Ai inputs go to the Bi outputs when enabled by $\overline{OE}1/\overline{OE}2$

These unity gain analog buffers achieve low propagation delays by having the output follow the input with a small offset. When the output reaches one V_{BE} off the rail, the PMOS pull-up is activated to drive the output the rest of the way. All inputs and outputs have Schottky clamp diodes to handle undershoot or overshoot noise suppression in unterminated applications. All outputs have ground bounce suppression (typically < 400mV), high drive output capability with almost immediate response to the input signal, and low output skew.

The I_{OL} current drive capability of a buffer/line driver is often interpreted as a measure of its ability to sink current in a dynamic sense. This may be true for CMOS buffer/ line drivers, but it is not true for the ML65T541. This is because their sink and source current capability depends on the voltage difference between the output and the input. The ML65T541 can sink or source more than 100mA to a load when the load is switching due to the fact that during the transition, the difference between the input and output is large. I_{OL} is only significant as a DC specification, and is 5mA.

Architectural Description

Until now, buffer/line drivers have been implemented in CMOS logic and made to be TTL compatible by sizing the input devices appropriately. In order to buffer large capacitances with CMOS logic, it is necessary to cascade an even number of inverters, each successive inverter larger than the preceding, eventually leading to an inverter that will drive the required load capacitance at the required frequency. Each inverter stage represents an additional delay in the gating process because in order for a single gate to switch, the input must slew more than half of the supply voltage. The best of these CMOS buffers has managed to drive a 50pF load capacitance with a delay of 3.2ns. Micro Linear has produced a dual quad buffer/line driver with a delay of less than 2ns by using a unique circuit architecture that does not require cascaded logic gates. The ML65T541 uses a feedback technique to produce an output that follows the input. If the output voltage is not close to the input, then the feedback circuitry will source or sink enough current to the load capacitance to correct the discrepancy.

The basic architecture of the ML65T541 is shown in Figure 5. It is implemented on a 1.5µm BiCMOS process.

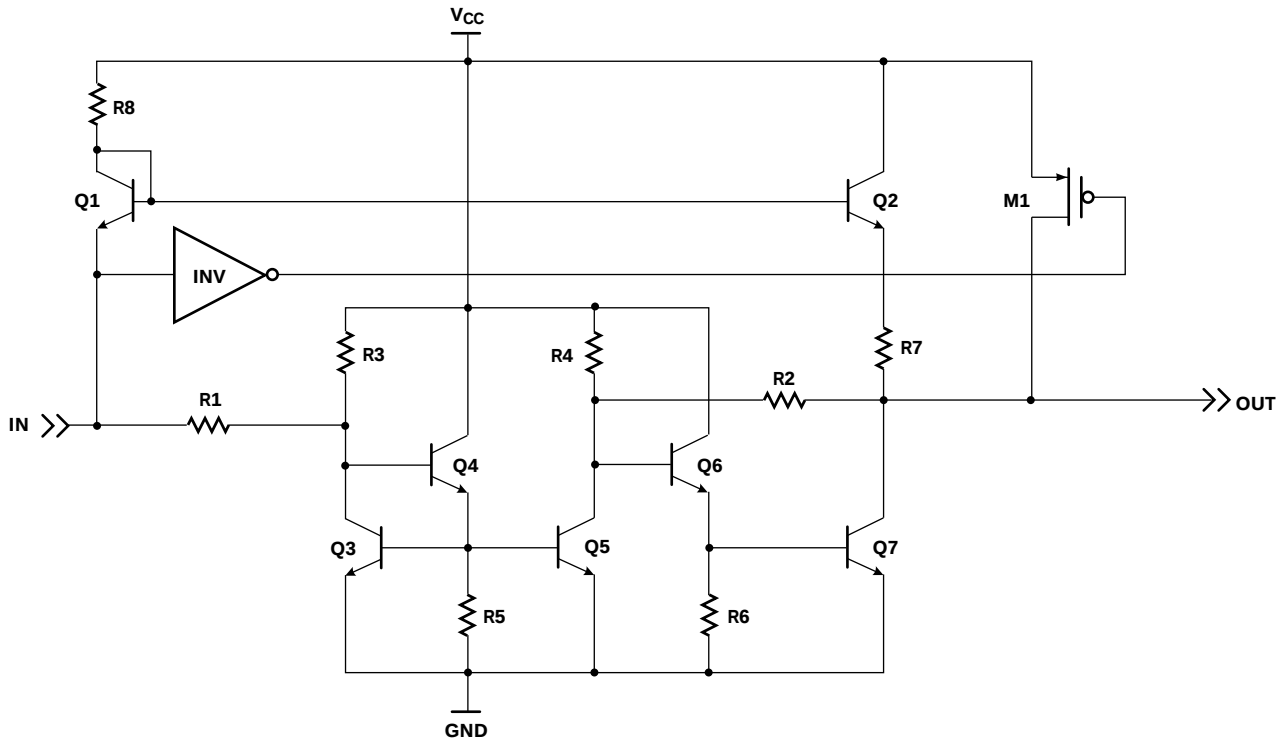


Figure 5. One buffer cell of the ML65T541

However, in this particular circuit, all of the active devices are NPNs — the fastest devices available in the process.

In this circuit, there are two paths to the output. One path sources current to the load capacitance when the signal is asserted, and the other path sinks current from the output when the signal is negated.

The assertion path is the emitter follower path consisting of the level shift transistor Q1, the output transistor Q2, the pull-up helper M1 (static R_{ON} ³ 200ý), and the bias resistor R8. It sources current to the output through the resistor R7 which is bypassed by another NPN (not shown) during fast input transients, and M1 pull-up drives the output toward the rail once the output reaches one V_{BE} within the rail. The negation path is a current differencing op amp connected in a follower configuration. The active components in this amplifier are transistors Q3–Q7. R3–R6 are bias resistors, and R1 and R2 are the feedback resistors. The key to understanding the operation of the current differencing op amp is to know that the current in transistors Q3 and Q5 are the same at all times and that the voltages at the bases of Q4 and Q6 are roughly the same. If the output is higher than the input, then an error current will flow through R2. This error current will flow into the base of Q6 and be multiplied by β squared to the collector of Q7, closing the loop. The larger the discrepancy between the output and input, the larger the feedback current, and the harder Q7 sinks current from the load capacitor.

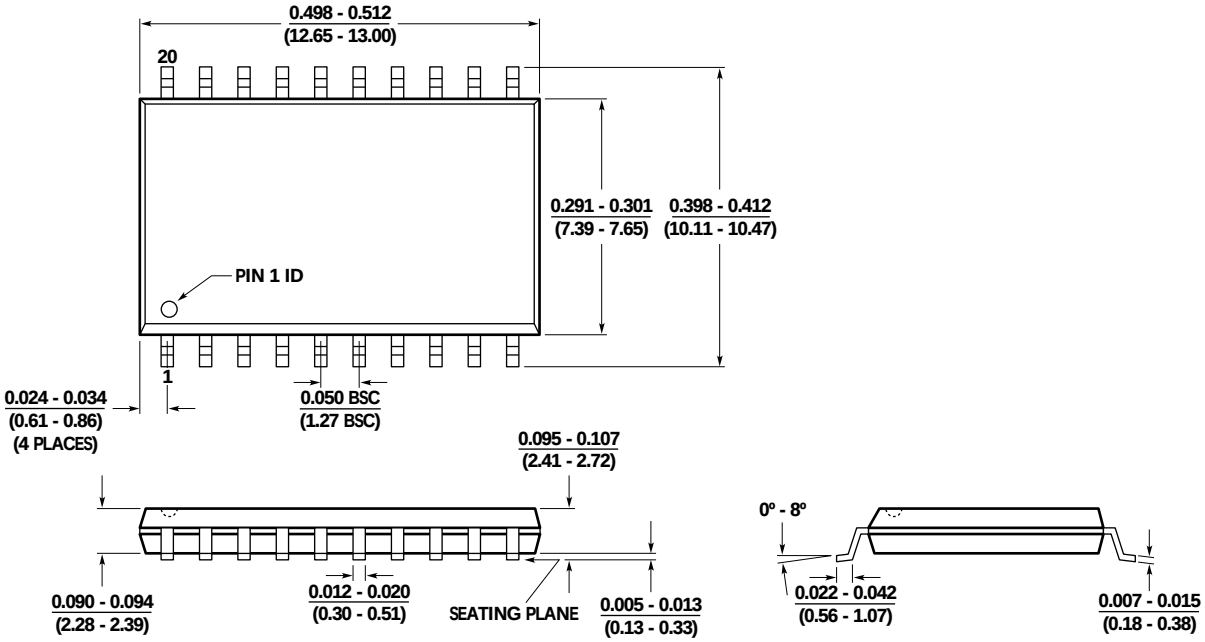
A number of MOSFETs are not shown in Figure 5. These MOSFETs are used to three-state dormant buffers. For instance, the feedback resistors R1 and R2 were implemented as resistive transmission gates to ensure that disabled buffers do not load the lines they are connected to. Similarly, there is a PMOS in series with R8 that is normally on but shuts off for disable. Other MOSFETs have been included to ensure that disabled buffers consume no power.

Applications

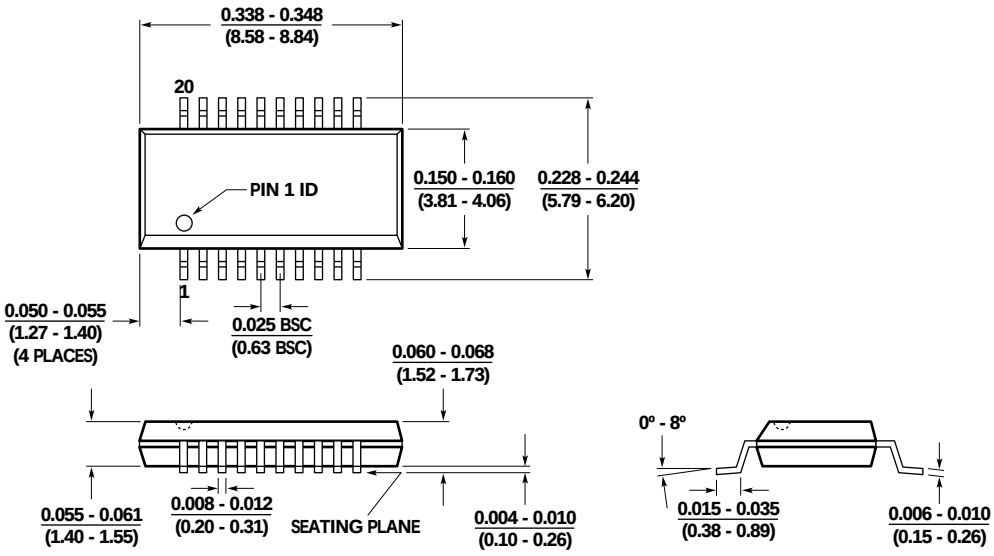
There are a wide variety of needs for an extremely fast buffers in high speed processor system designs like Pentium, PowerPC, Mips, Sparc, Alpha and other RISC processors. These applications are either in the cache memory area or the main memory (DRAM) area. In addition, fast buffers find applications in high speed graphics and multimedia applications. The high capacitive loading due to multiplexed address lines on the system bus demand external buffers to take up the excess drive current. The needed current to skew the transitions between rise and fall times must be done without adding excessive propagation delay. The ML65T541 is equipped with Schottky diodes to clean up ringing from overshoot and undershoot caused by reflections in unterminated board traces.

Physical Dimensions inches (millimeters)

Package: S20
20-Pin SOIC



Package: K20
20-Pin QSOP



Ordering Information

Part Number	Speed	Temperature Range	Package
ML65T541CK	2.0ns	0°C to 70°C	20-Pin QSOP (K20)
ML65T541CS	2.0ns	0°C to 70°C	20-Pin SOIC (S20)