16-bit registered transceiver; (3-State)

74ABT16952
74ABTH16952

FEATURES

- Two 8-bit registered transceivers
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16952 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Independent registers for A and B buses
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16952 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16952 is a dual octal registered transceiver. Two 8-bit registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (nCPXX) provided that the Clock Enable ($n\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($n\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

Two options are available, 74ABT16952 which does not have the bus-hold feature and 74ABTH16952 which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx or nCPAB to nBx	C_L = 50pF; V_{CC} = 5V	2.8 2.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5V	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16952 DL	BT16952 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16952 DGG	BT16952 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16952 DL	BH16952 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16952 DGG	BH16952 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55 18, 22	1CPAB / 1CPBA 2CPAB / 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	$1\overline{CEAB}$ / $1\overline{CEBA}$ $2\overline{CEAB}$ / $2\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1A0 – 1A7 2A0 – 2A7	Data inputs/outputs (A side)
1, 56 8, 29	1B0 – 1B7 2B0 – 2B7	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 45, 53	$1\overline{OEAB}$ / $1\overline{OEBA}$ $2\overline{OEAB}$ / $2\overline{OEBA}$	Output enable inputs
4, 17, 30, 43	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

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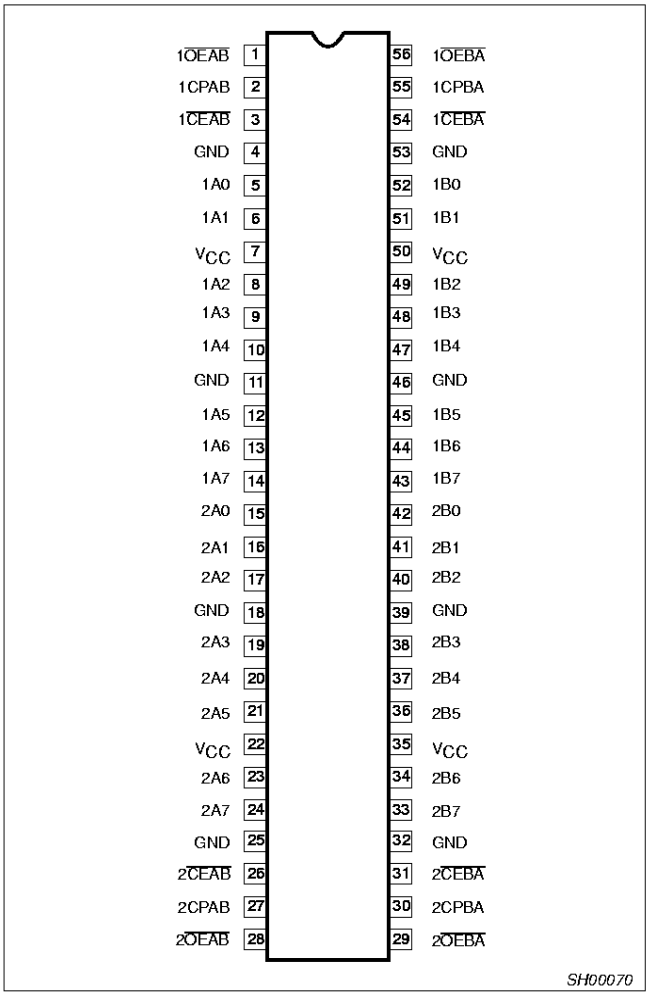
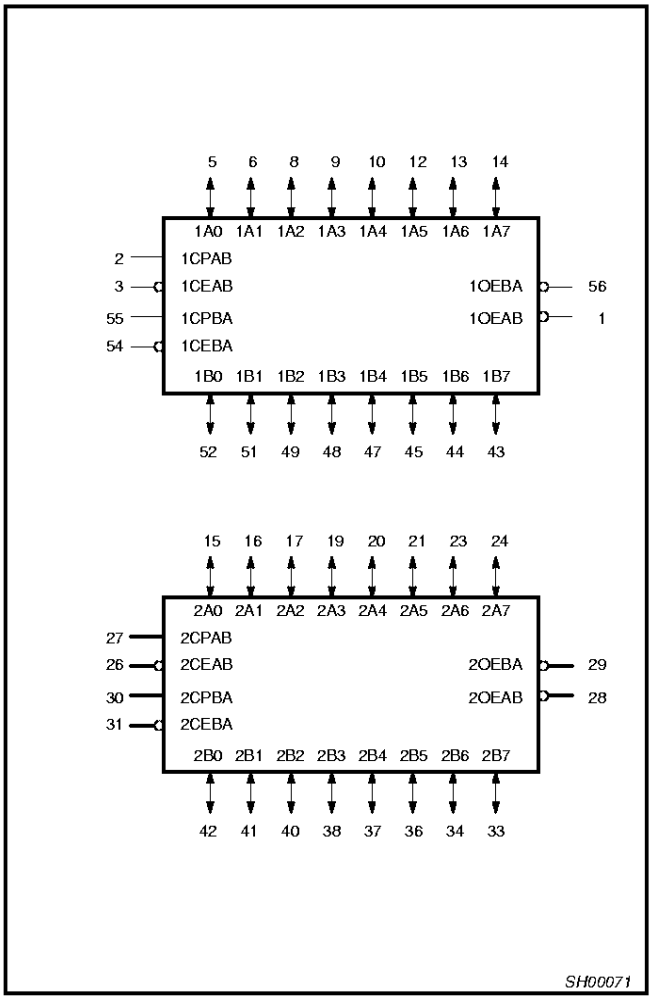
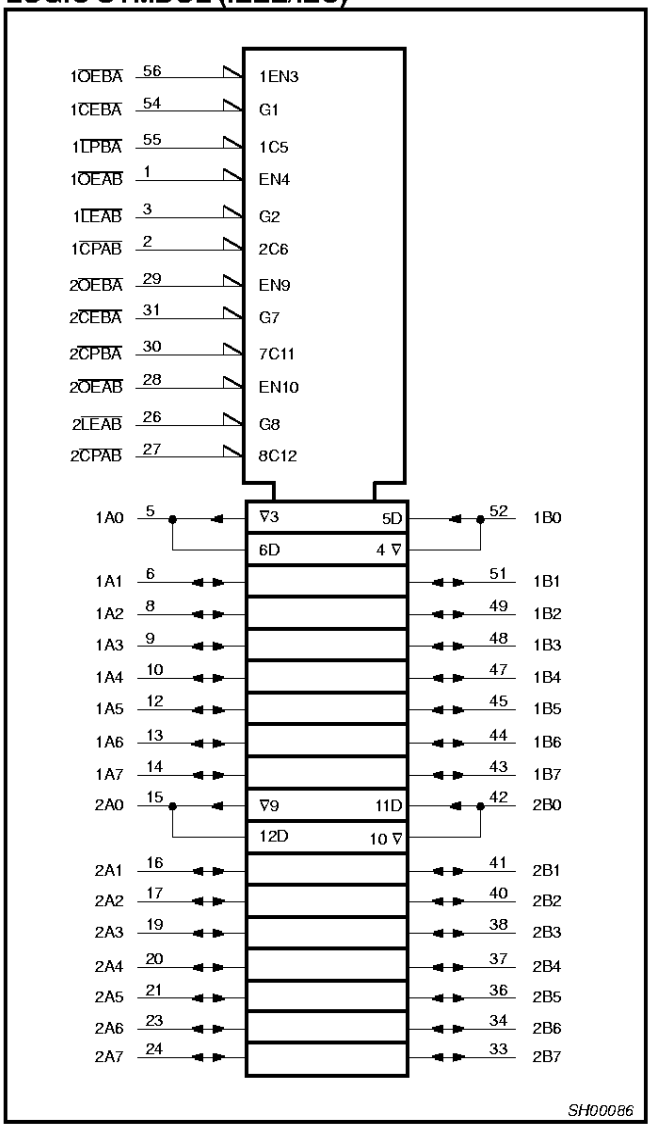
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL	OPERATING
nAx or nBx	nCPXX	nCEXX	Q	MODE
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

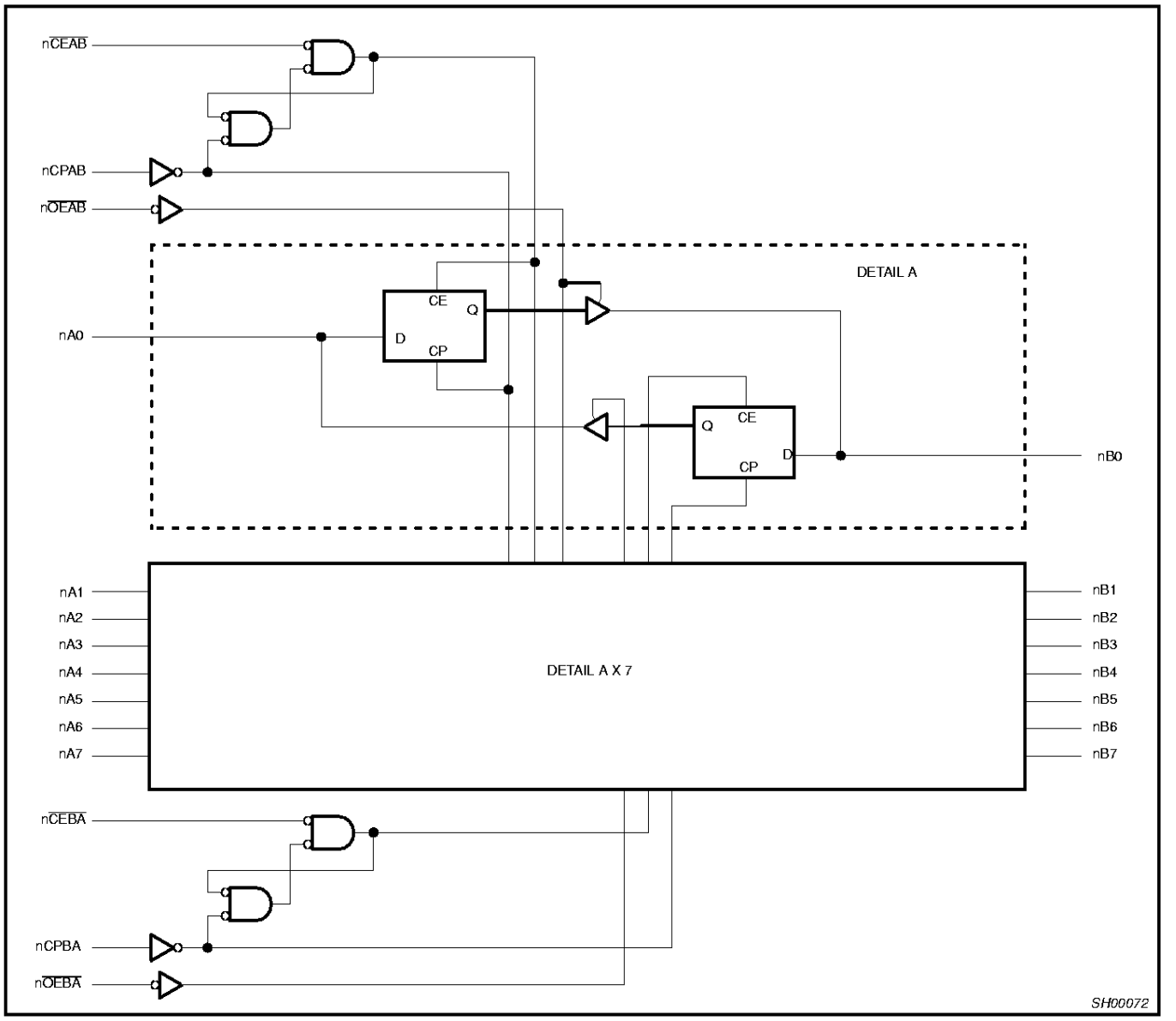
H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	nAx or nBx	OPERATING
nOEXX	Q	OUTPUTS	MODE
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_{OL} = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current — Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A inputs 74ABTH16952	V_{CC} = 4.5V, V_I = 0.8V	50			50		µA
		V_{CC} = 4.5V; V_I = 2.0V	–75			–75		µA
I_{OFF}	Power-off leakage current	V_{CC} = 0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = Don't care		±5.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{cc}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	1.5		1.5	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	1.5		1.5	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16952	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		5	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16952	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		100	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

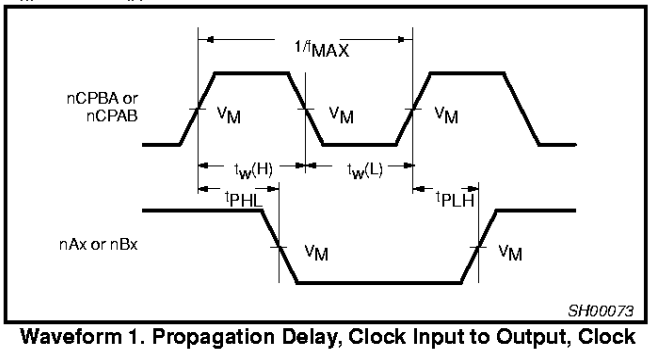
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	150			150		MHz
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx, nCPAB to nBx	1	1.0 1.0	2.8 2.3	3.9 3.9	1.0 1.0	4.3 4.3	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OEBA}$ to nAx, $n\overline{OEAB}$ to nBx	3 4	1.0 1.0	2.5 2.2	3.8 3.8	1.0 1.0	4.6 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OEBA}$ to nAx, $n\overline{OEAB}$ to nBx	3 4	1.7 1.3	3.4 2.6	4.4 3.9	1.7 1.3	5.2 4.2	ns

AC SETUP REQUIREMENTS

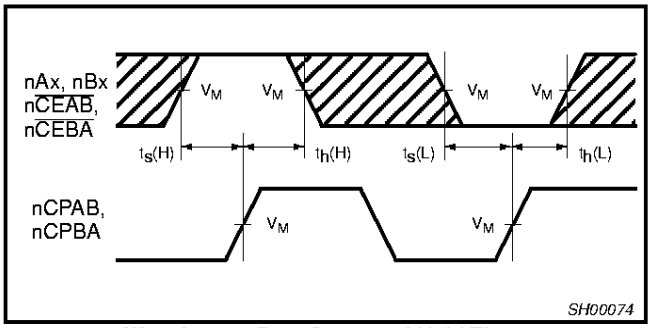
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C V_{CC} = +5.0V		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_S(H)$ $t_s(L)$	Setup time nAx to nCPAB or nBx to nCPBA	2	1.2 1.5	0.9 1.2	1.2 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nCPAB or nBx to nCPBA	2	0.0 0.0	–1.2 –0.9	0.0 0.0	ns
$t_s(H)$ $t_s(L)$	Setup time $n\overline{CEAB}$ to nCPAB, $n\overline{CEBA}$ to nCPBA	2	1.2 1.6	0.9 1.1	1.2 1.6	ns
$t_h(H)$ $t_h(L)$	Hold time $n\overline{CEAB}$ to nCPAB, $n\overline{CEBA}$ to nCPBA	2	0.0 0.0	–1.1 –0.9	0.0 0.0	ns
$t_w(H)$ $t_w(L)$	nCPAB or nCPBA pulse width, High or Low	1	3.3 2.5	2.6 1.0	3.3 2.5	ns

AC WAVEFORMS

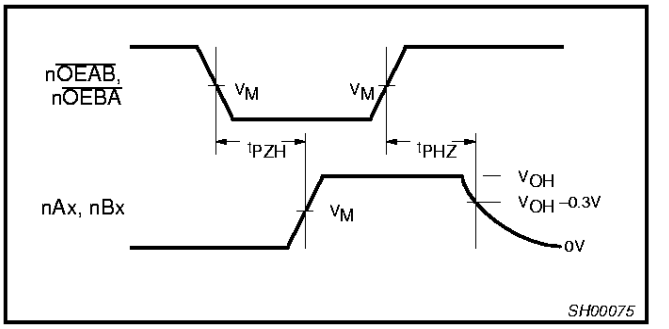
V_M = 1.5V, V_{IN} = GND to 3.0V



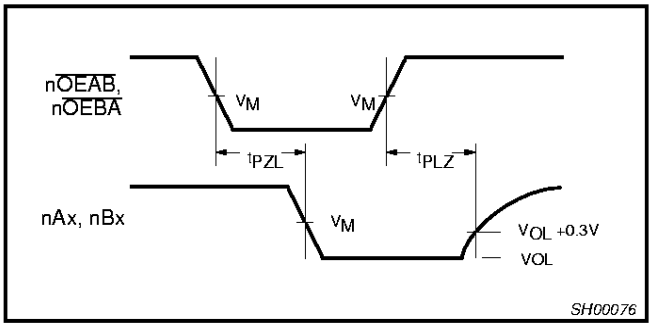
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

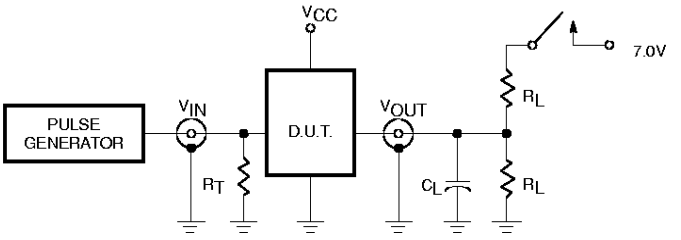


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

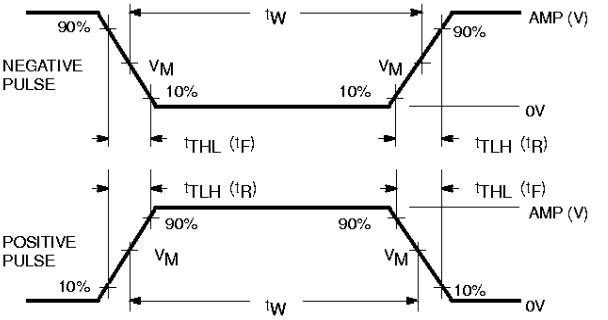


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018