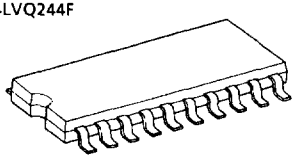
TC74LVQ240F/FW/FS, TC74LVQ241F/FW/FS TC74LVQ244F/FW/FS

OCTAL BUS BUFFER
TC74LVQ240 INVERTED, 3-STATE OUTPUTS
TC74LVQ241 NON-INVERTED, 3-STATE OUTPUTS
TC74LVQ244 NON-INVERTED, 3-STATE OUTPUTS

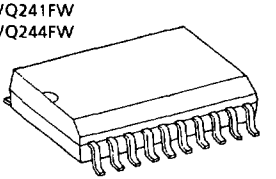
The TC74LVQ240, 241 and 244 are high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation.
The TC74LVQ240 is an inverting 3-state buffer having two active-low output enables. The TC74LVQ241 and TC74LVQ244 are non-inverting 3-state buffers that differ only in that the LVQ241 has one active-high and one active-low output enable, and the LVQ244 has two active-low output enables.
These devices are designed to be used with 3-state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74LVQ240F
TC74LVQ241F
TC74LVQ244F



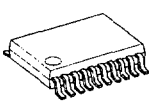
SOP20-P-300

TC74LVQ240FW
TC74LVQ241FW
TC74LVQ244FW



SOL20-P-300

TC74LVQ240FS
TC74LVQ241FS
TC74LVQ244FS



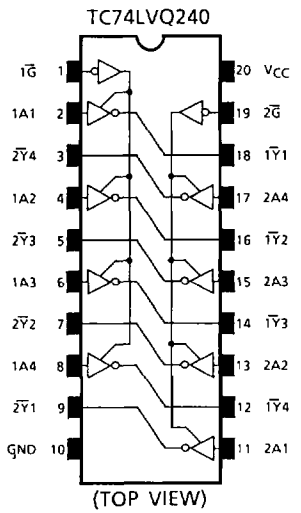
SSOP20-P-225A

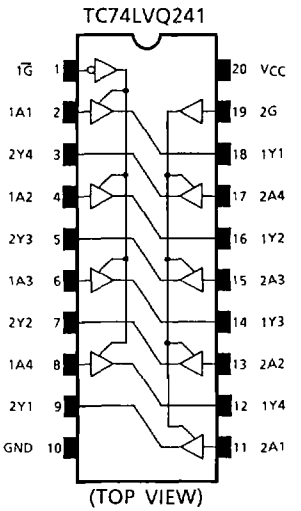
Weight SOP20-P-300 : 0.22g (Typ.)
SOL20-P-300 : 0.46g (Typ.)
SSOP20-P-225A : 0.09g (Typ.)

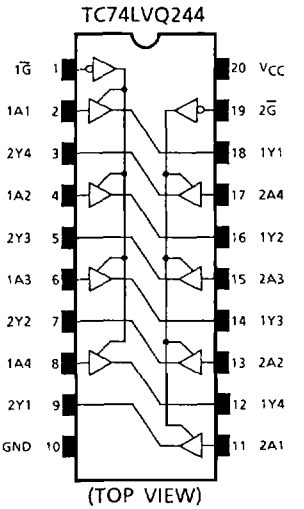
FEATURES

- High speed : $t_{pd} = 5.4ns$ (Typ) ($V_{CC} = 3.3V$)
- Low power dissipation : $I_{CC} = 4\mu A$ (Max.) ($Ta = 25°C$)
- Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$)
  $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)
- Symmetrical output impedance
  : $|I_{OH}| = I_{OL} = 12mA$ (Min.)
- Balanced propagation delays
  : $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74HC240/241/244

PIN ASSIGNMENT







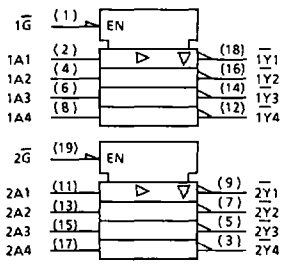
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	G△	A_n	Y_n	$\overline{Y}_n$△△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

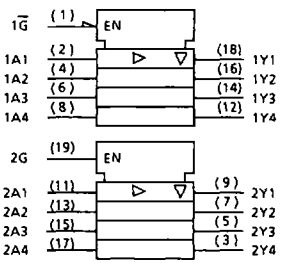
△ : for TC74LVQ241 only
△△ : for TC74LVQ240 only
X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOL

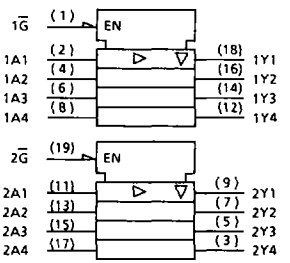
TC74LVQ240



TC74LVQ241



TC74LVQ244



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} / Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10s	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt / dv	0~100	ns / V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Input Voltage	"H" Level	V_{IH}			3.0	2.0	—	—	2.0	—	V
	"L" Level	V_{IL}			3.0	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-50\mu A$	3.0	2.9	3.0	—	2.9	—	V
				$I_{OH}=-12mA$	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=50\mu A$	3.0	—	0.0	0.1	—	0.1	
				$I_{OL}=12mA$	3.0	—	—	0.36	—	0.44	
3-State Output Off-State Current		I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		3.6	—	—	±0.5	—	±5.0	μA
Input Leakage Current		I_{IN}	$V_{IN}=V_{CC}$ or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current		I_{CC}	$V_{IN}=V_{CC}$ or GND		3.6	—	—	4.0	—	40.0	μA

AC characteristics (Input $t_r=t_f=3ns$, $C_L=50pF$, $R_L=500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Propagation Delay Time (TC74LVQ240)	t_{pLH} t_{pHL}		2.7	—	7.2	14.1	1.0	15.0	ns
			3.3±0.3	—	6.0	10.0	1.0	10.5	
Propagation Delay Time (TC74VLQ241/244)	t_{pLH} t_{pHL}		2.7	—	7.8	13.4	1.0	15.0	ns
			3.3±0.3	—	6.5	9.5	1.0	10.5	
Output Enable Time	t_{pZL} t_{pZH}		2.7	—	9.5	18.3	1.0	19.0	ns
			3.3±0.3	—	7.9	13.0	1.0	13.5	
Output Disable Time	t_{pLZ} t_{pHZ}		2.7	—	7.2	19.0	1.0	20.0	ns
			3.3±0.3	—	6.0	13.5	1.0	14.0	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	—	—	1.5	—	1.5	ns
			3.3±0.3	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)		—	5	10	—	10	pF
Output Capacitance	C_{OUT}			—	10	—	—	—	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		—	30	—	—	—	pF

(Note 1) Parameter guaranteed by design.
($t_{osLH}=|t_{pLHm}-t_{pLHn}|$, $t_{osHL}=|t_{pHLm}-t_{pHLn}|$)

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :

$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/8$ (per bit)

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V