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## NTE74LS33 Integrated Circuit TTL – Quad 2–Input Positive NOR Buffer with Open–Collector Outputs

**Description:**

The NTE74LS33 contains four independent 2–Input NOR buffer gates with open–collector outputs in a 14–Lead plastic DIP type package. Open–collector outputs require resistive pull–up to perform logically but can deliver higher  $V_{OH}$  levels and are commonly used in wired–AND applications.

**Absolute Maximum Ratings:** (Note 1)

|  |                 |
|--|-----------------|
| Supply Voltage, $V_{CC}$ .....             | 7V              |
| DC Input Voltage, $V_{IN}$ .....           | 7V              |
| Off–State Output Voltage .....             | 7V              |
| Operating Temperature Range, $T_A$ .....   | 0°C to +70°C    |
| Storage Temperature Range, $T_{stg}$ ..... | –65°C to +150°C |

Note 1. Unless otherwise specified, all voltages are referenced to GND.

**Recommended Operating Conditions:**

| Parameter                   | Symbol   | Min  | Typ | Max  | Unit |
|-----------------------------|----------|------|-----|------|------|
| Supply Voltage              | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V    |
| High–Level Input Voltage    | $V_{IH}$ | 2.0  | –   | –    | V    |
| Low–Level Input Voltage     | $V_{IL}$ | –    | –   | 0.8  | V    |
| High–Level Output Voltage   | $V_{OH}$ | –    | –   | 5.5  | V    |
| Low–Level Output Current    | $I_{OL}$ | –    | –   | 24   | mA   |
| Operating Temperature Range | $T_A$    | 0    | –   | +70  | °C   |

**Electrical Characteristics:** (Note 2, Note 3)

| Parameter                 | Symbol   | Test Conditions  | Min | Typ  | Max  | Unit |
|---------------------------|----------|--|-----|------|------|------|
| Input Clamp Voltage       | $V_{IK}$ | $V_{CC} = \text{MIN}, I_I = -18\text{mA}$                        | –   | –    | –1.5 | V    |
| High Level Output Current | $I_{OH}$ | $V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{OH} = 5.5\text{V}$  | –   | –    | 0.25 | mA   |
| Low Level Output Voltage  | $V_{OL}$ | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 12\text{mA}$ | –   | 0.25 | 0.4  | V    |
|                           |          | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 24\text{mA}$ | –   | 0.35 | 0.5  | V    |
| Input Current             | $I_I$    | $V_{CC} = \text{MAX}, V_I = 7\text{V}$                           | –   | –    | 0.1  | mA   |

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at  $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ .

**Electrical Characteristics (Cont'd):** (Note 2, Note 3)

| Parameter                 | Symbol    | Test Conditions                          | Min | Typ | Max  | Unit          |
|---------------------------|-----------|--|-----|-----|------|---------------|
| High Level Input Current  | $I_{IH}$  | $V_{CC} = \text{MAX}, V_I = 2.7\text{V}$ | -   | -   | 20   | $\mu\text{A}$ |
| Low Level Input Current   | $I_{IL}$  | $V_{CC} = \text{MAX}, V_I = 0.4\text{V}$ | -   | -   | -0.4 | mA            |
| High Level Supply Current | $I_{CCH}$ | $V_{CC} = \text{MAX}, V_I = 0$           | -   | 1.8 | 3.6  | mA            |
| Low Level Supply Current  | $I_{CCL}$ | $V_{CC} = \text{MAX}, \text{Note 4}$     | -   | 6.9 | 13.8 | mA            |

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 3. All typical values are at  $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ .

Note 4. One input at 4.5V, all others at GND.

**Switching Characteristics:** ( $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$  unless otherwise specified)

| Parameter  | Symbol    | Test Conditions                      | Min | Typ | Max | Unit |
|--|-----------|--------------------------------------|-----|-----|-----|------|
| Propagation Delay Time<br>From A or B Input to Y Output) | $t_{PLH}$ | $R_L = 667\Omega, C_L = 45\text{pF}$ | -   | 20  | 32  | ns   |
|  | $t_{PHL}$ |                                      | -   | 18  | 28  | ns   |

**Truth Table (Each Gate):**

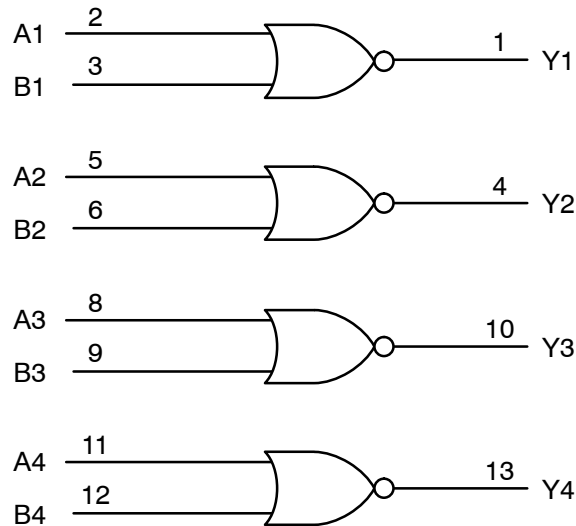
| Inputs |   | Output |
|--------|---|--------|
| A      | B | Y      |
| H      | X | L      |
| X      | H | L      |
| L      | L | H      |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

**Logic Diagram**



$$Y = \overline{A} \bullet \overline{B} \text{ or } Y = \overline{A} + \overline{B}$$

Pin14 =  $V_{CC}$   
Pin7 = GND

### Pin Connection Diagram

