FAST 74F755
Register

FAST Products

Octal MailBox Register With Ready Flag (3-State)

Product Specification

FEATURES

- **Flag set on Write signal (if desired)**
- **Automatic flag set upon Read signal**
- **Pen collector flag status output**
- **Flag status can be read via data bus**
- **300 mil 24 pin Slim DIP plastic package option**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F755	180MHz	60mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F755N
24-Pin Plastic SOL	N74F755D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

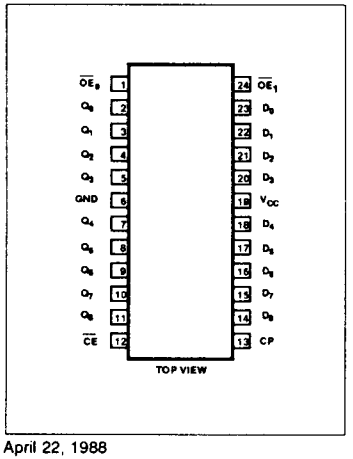
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_8	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/3.0	20µA/1.8mA
$\overline{CE}$	Chip Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
Q_8	Open Collector output	OC/ 40	OC/24mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

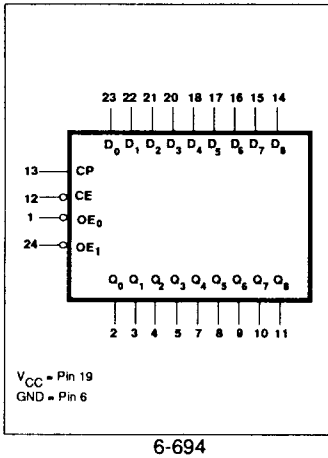
DESCRIPTION

The 74F755 is an octal three state register with simple handshaking logic. Data is latched into and read from the part in the same manner as the 'F374 or other octal registers with the exception that the 'F755 has a Clock Enable pin. Handshaking can be performed in either a polled or interrupt environment by using the D_8 input and the Q_7 or Q_8 output. D_8 is latched along with the other data bits on the rising edge of the clock, but is handled differently on the output. The status of this bit can be sampled on the Q_8 open collector output and used as an interrupt or other control function. The status of D_8 can also be sampled on the Q_7 output with the appropriate combination of $\overline{OE}_0$ and $\overline{OE}_1$ for polled operation. The D_8 register is automatically reset when Q_0-Q_7 are sampled, resetting the handshaking for the next cycle. The 'F755 is equipped with a true Clock Enable ($\overline{CE}$) pin. There are no functional restrictions on the use of the $\overline{CE}$ pin. $\overline{CE}$ may be cycled with the clock input either Low or High with no false clocks generated. The 'F755 can serve as a single chip communications channel with simple handshaking, or two can be used for a bidirectional channel.

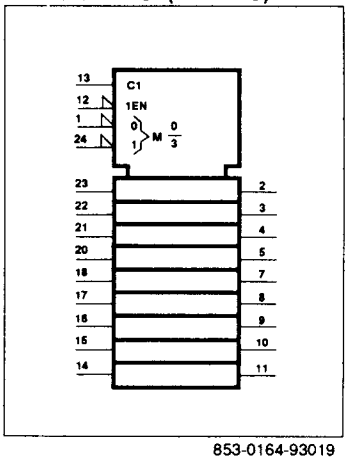
PIN CONFIGURATION



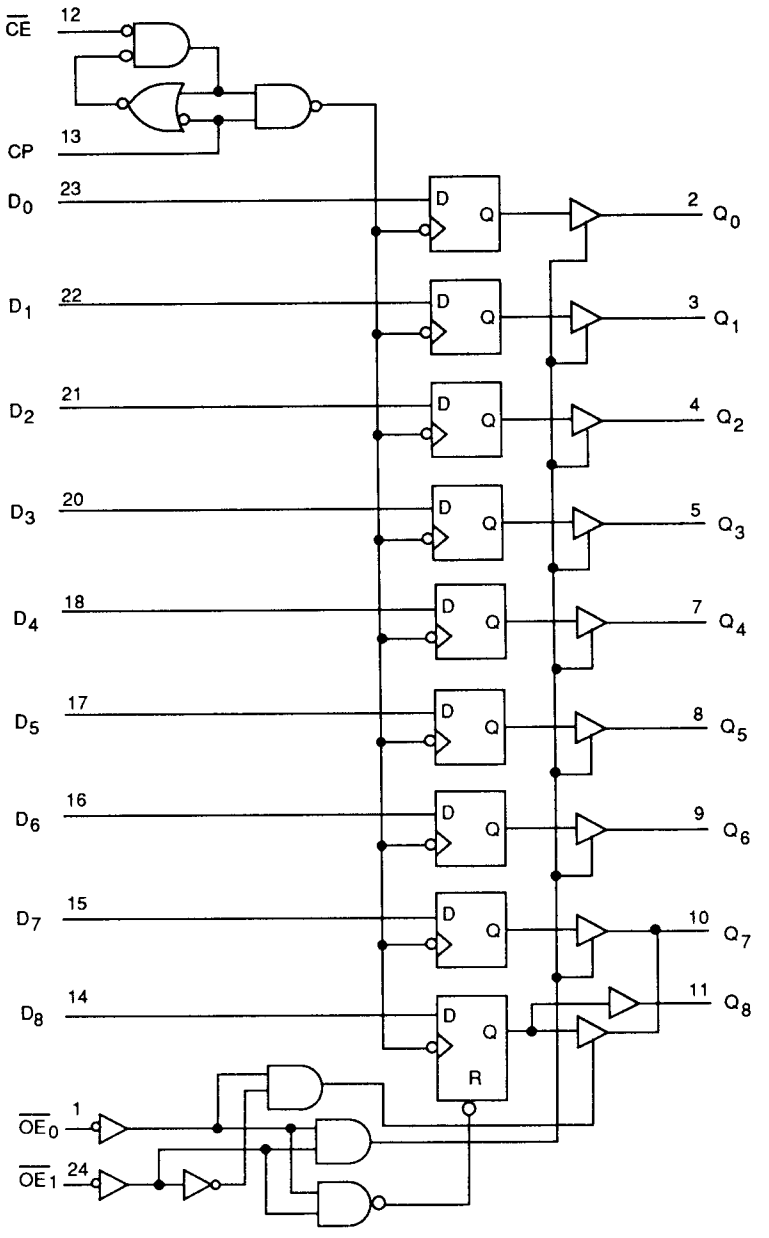
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						INTERNAL REGISTERS		OUTPUTS			OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{CE}$	CP	D_0-D_7	D_8	Q_0-Q_7	Q_8	Q_0-Q_6	Q_7	Q_8	
H	X	L	↧	X	X	Q_0-Q_7	Q_8	Z	Z	Q_8	Hold and Read Q_8
H	X	H	X	X	X	Q_0-Q_7	Q_8	Z	Z	Q_8	
L	H	L	↧	X	X	Q_0-Q_7	Q_8	Z	Q_8	Q_8	
L	H	H	X	X	X	Q_0-Q_7	Q_8	Z	Q_8	Q_8	
L	L	L	↧	X	X	Q_0-Q_7	L	Q_0-Q_6	Q_7	L	Hold and Read (Q_0-Q_7) and reset Q_8
L	L	H	X	X	X	Q_0-Q_7	L	Q_0-Q_6	Q_7	L	
H	X	L	↑	D_0-D_7	D_8	D_0-D_7	D_8	Z	Z	D_8	Load (D_0-D_8)
L	H	L	↑	D_0-D_7	D_8	D_0-D_7	D_8	Z	D_8	D_8	
L	L	L	↑	D_0-D_7	X	D_0-D_7	L	D_0-D_6	D_7	L	Load (D_0-D_7) and reset Q_8

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↧ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High level output voltage	Q_8 only			4.5	V
I_{OH}	High-level output current	Q_0-Q_7			-3	mA
I_{OL}	Low-level output current				24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	Q_8 only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Q_0-Q_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=MAX	±10%VCC	2.4			V
					±5%VCC	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=MAX	±10%VCC		0.35	0.50	V
					±5%VCC		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 5.5V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					-600	µA
		CP						-1.8	mA
I_{OZH}	Off-state output current High-level voltage applied	Q_0-Q_7	V_{CC} = MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	70	mA
		I_{CCL}					65	90	mA
		I_{CCZ}					60	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

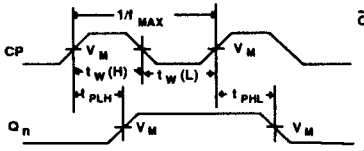
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	165	180		160		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0-Q_7	Waveform 1	3.0 4.5	5.0 6.5	8.0 9.5	2.5 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_8	Waveform 1	7.5 5.0	9.5 6.5	12.0 9.5	7.5 4.5	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_1$ to Q_7	Waveform 2	6.0 6.5	7.5 8.5	10.5 11.0	5.0 6.5	11.5 11.5	ns
t_{PHL}	Propagation delay OE_n to Q_8 (reset)	Waveform 2	9.0	11.5	15.0	8.0	17.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_0$ to Q_0-Q_7	Waveform 4 Waveform 5	7.0 7.5	9.0 10.0	12.0 13.0	6.0 6.5	13.0 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ to Q_0-Q_7	Waveform 4 Waveform 5	3.5 4.0	5.5 6.0	8.0 9.0	2.5 3.5	9.0 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_1$ to Q_0-Q_7	Waveform 4 Waveform 5	5.5 6.0	7.5 8.0	10.5 11.0	4.5 5.5	11.5 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_1$ to Q_0-Q_7	Waveform 4 Waveform 5	3.0 3.5	5.0 5.5	7.5 8.5	2.5 3.0	8.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_0$ to Q_7	Waveform 4 Waveform 5	9.5 10.5	11.0 12.5	14.0 15.0	8.5 9.5	16.0 17.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ to Q_7	Waveform 4 Waveform 5	3.5 3.5	5.0 5.5	8.0 8.0	2.5 3.5	8.5 8.5	ns

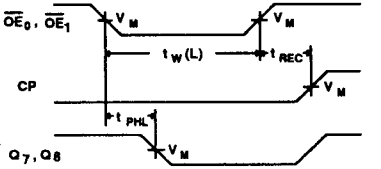
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 3	3.5 3.0			4.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{CE}$ to CP	Waveform 3	0.0 0.0			0.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CE}$ to CP	Waveform 3	2.0 3.0			2.5 3.0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1	3.0 3.5			3.0 4.0		ns
t_w(L)	$\overline{OE}_0$ Pulse width,Low	Waveform 2	6.5			8.5		ns
t_w(L)	$\overline{OE}_1$ Pulse width, Low	Waveform 2	5.5			6.5		ns
t_{REC}	Recovery time, $\overline{OE}_n$ to CP	Waveform 2	5.0			5.5		ns

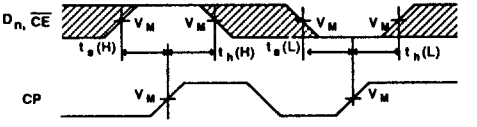
AC WAVEFORMS



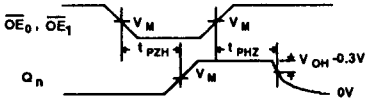
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



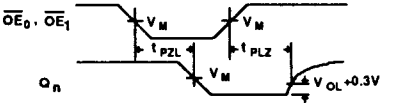
Waveform 2. Output Enables Pulse Width, Output Enables to Q8 Output Delay and Output Enables to Clock ad Chip Enable Recovery Time



Waveform 3. Data Setup And Hold Times



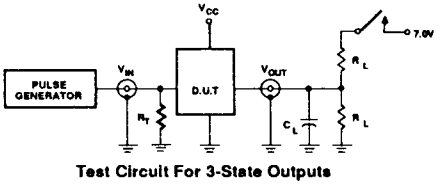
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

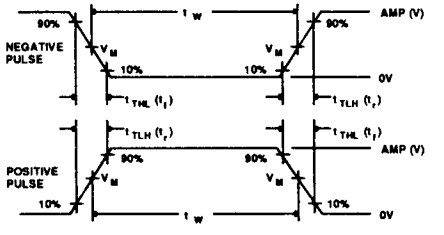
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns