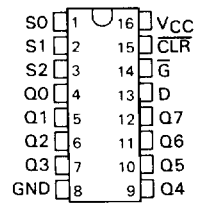
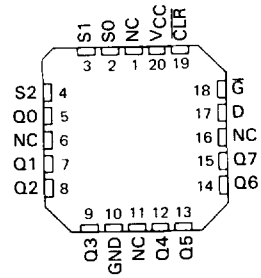
- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPS
- Dependable Texas Instruments Quality and Reliability

SN54ALS259 . . . J PACKAGE
SN74ALS259 . . . N PACKAGE
(TOP VIEW)




SN54ALS259 . . . FH PACKAGE
SN74ALS259 . . . FN PACKAGE
(TOP VIEW)




NC – No internal connection

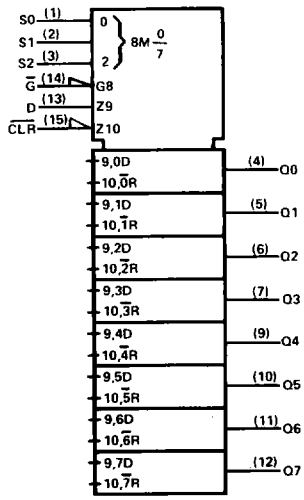
## description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54ALS259 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS259 will be characterized for operation from 0°C to 70°C.

## logic symbol




Pin numbers shown are for J and N packages.

**FUNCTION TABLE**

| INPUTS $\overline{CLR}$ | INPUTS $\overline{G}$ | OUTPUT OF ADDRESSED LATCH | EACH OTHER OUTPUT | FUNCTION |
|---|---|---|---|---|
| H | L | D | $Q_{i0}$ | Addressable Latch |
| H | H | $Q_{i0}$ | $Q_{i0}$ | Memory |
| L | L | D | L | 8-Line Demultiplexer |
| L | H | L | L | Clear |

D = the level at the data input.
$Q_{i0}$ = the level of $Q_i$ (i = 0, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

**LATCH SELECTION TABLE**

| SELECT INPUTS S2 | S1 | S0 | LATCH ADDRESSED |
|---|---|---|---|
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |