

## BCD-to-Seven Segment Decoder

The MC14558B decodes 4-bit binary coded decimal data dependent on the state of auxiliary inputs, Enable and  $\overline{RBI}$ , and provides an active-high seven-segment output for a display driver.

An auxiliary input truth table is shown, in addition to the BCD to seven-segment truth table, to indicate the functions available with the two auxiliary inputs.

Leading Zero blanking is easily obtained with an external flip-flop in time division multiplexed systems displaying most significant decade first.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Segment Blanking for All Illegal Input Combinations
- Lamp Test Function
- Capability for Suppression of Non-Significant Zeros
- Lamp Intensity Function
- Capable of Driving Two Low-power TTL Loads. One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages referenced to $V_{SS}$ )

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}$	-0.5 to +18	V
Input Voltage, All Inputs	$V_{in}$	-0.5 to $V_{DD} + 0.5$	V
DC Input Voltage, per Pin	$I_{in}$	$\pm 10$	mAdc
Operating Temperature Range	$T_A$	-55 to +125	$^{\circ}C$
Power Dissipation, per Package†	$P_D$	500	mW
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}C$

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

Ceramic "L" Packages: - 12 mW/ $^{\circ}C$  From 100 $^{\circ}C$  To 125 $^{\circ}C$

### AUXILIARY INPUT TRUTH TABLE

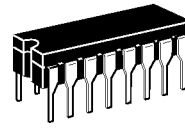
Enable Pin 3	$\overline{RBI}$ Pin 5	BCD Input Code	$\overline{RBO}$ Pin 4	Function Performed
0	0	X	0	Lamp Test
0	1	X	1	Blank Segments
1	1	0	1	Display Zero
1	0	0	0	Blank Segments
1	X	1-9	1	1-9 Displayed

X = Don't Care

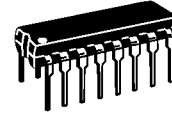
$\overline{RBI}$  = Ripple Blanking Input

$\overline{RBO}$  = Ripple Blanking Output

## MC14558B



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



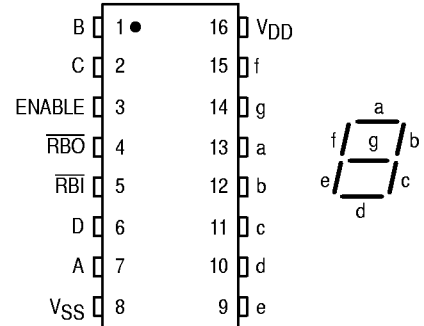
**D SUFFIX**  
SOIC  
CASE 751B

### ORDERING INFORMATION

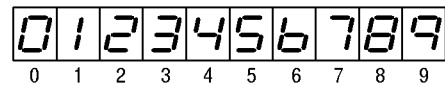
MC14XXXBCP Plastic  
MC14XXXBCL Ceramic  
MC14XXXBD SOIC

$T_A = -55^{\circ}C$  to  $125^{\circ}C$  for all packages.

### PIN ASSIGNMENT



### DISPLAY



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ #	Max	Min	Max			
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc		
		10	—	0.05	—	0	0.05	—	0.05			
		15	—	0.05	—	0	0.05	—	0.05			
	"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95		—	Vdc
			10	9.95	—	9.95	10	—	9.95		—	
			15	14.95	—	14.95	15	—	14.95		—	
Input Voltage	"0" Level V <sub>IL</sub> (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc		
		10	—	3.0	—	4.50	3.0	—	3.0			
		15	—	4.0	—	6.75	4.0	—	4.0			
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5		—	Vdc
			10	7.0	—	7.0	5.50	—	7.0		—	
			15	11	—	11	8.25	—	11		—	
Output Drive Current	Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA <sub>dc</sub>	
			10	-0.64	—	-0.51	-0.88	—	-0.36	—		
			15	-1.6	—	-1.3	-2.25	—	-0.9	—		
			15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—		mA <sub>dc</sub>
			10	1.6	—	1.3	2.25	—	0.9	—		
15	4.2	—	3.4	8.8	—	2.4	—	—				
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA <sub>dc</sub>		
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF		
Quiescent Current (Per Package) V <sub>in</sub> = 0 or V <sub>DD</sub> I <sub>out</sub> = 0 μA	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μA <sub>dc</sub>		
		10	—	10	—	0.010	10	—	300			
		15	—	20	—	0.015	20	—	600			
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.2 μA/kHz) f + I <sub>DD</sub>							μA <sub>dc</sub>		
		10	I <sub>T</sub> = (2.4 μA/kHz) f + I <sub>DD</sub>									
		15	I <sub>T</sub> = (3.6 μA/kHz) f + I <sub>DD</sub>									

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min @ V<sub>DD</sub> = 5.0 V  
 2.0 V min @ V<sub>DD</sub> = 10 V  
 2.5 V min @ V<sub>DD</sub> = 15 V

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V<sub>DD</sub> in V, and f in kHz is input frequency.

\*\*The formulas given are for the typical characteristics only at 25°C.

**This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V<sub>in</sub> and V<sub>out</sub> be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>).**

**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ ; see Figure 1)

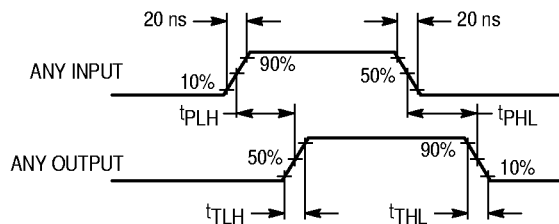
Characteristic	Symbol	V <sub>DD</sub>	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 495 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 187 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 120 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	580 220 145	1160 440 230	ns
Propagation Delay Time $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 695 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 242 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 160 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	780 275 185	1560 550 370	ns

\* The formulae given are for the typical characteristics only.

**TRUTH TABLE**

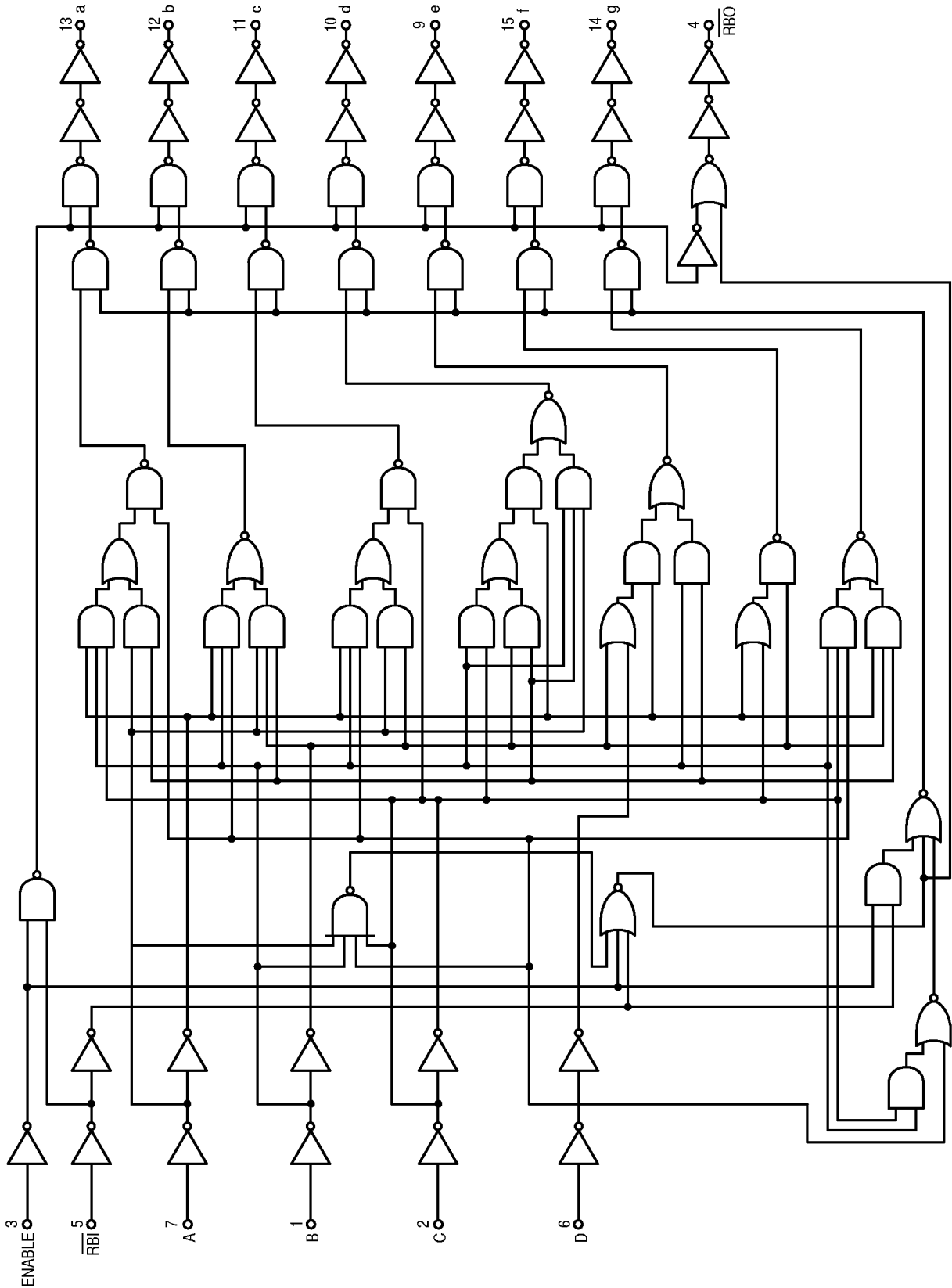
Inputs						Outputs*								
Enable Pin 3	$\overline{\text{RBI}}$ Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14	$\overline{\text{RBO}}$ Pin 4	Display
1	1	0	0	0	0	1	1	1	1	1	1	0	1	0
1	X	0	0	0	1	0	0	0	0	1	1	0	1	1
1	X	0	0	1	0	1	1	0	1	1	0	1	1	2
1	X	0	0	1	1	1	1	1	1	0	0	1	1	3
1	X	0	1	0	0	0	1	1	0	0	1	1	1	4
1	X	0	1	0	1	1	0	1	1	0	1	1	1	5
1	X	0	1	1	0	0	0	1	1	1	1	1	1	6
1	X	0	1	1	1	1	1	1	0	0	0	0	1	7
1	X	1	0	0	0	1	1	1	1	1	1	1	1	8
1	X	1	0	0	1	1	1	1	0	0	1	1	1	9
1	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank
0	0	X	X	X	X	1	1	1	1	1	1	1	0	8
0	1	X	X	X	X	0	0	0	0	0	0	0	1	Blank

\* All non-valid BCD input codes produce a blank display.  
 X = Don't Care



**Figure 1. Signal Waveforms**

LOGIC DIAGRAM



## TYPICAL APPLICATIONS

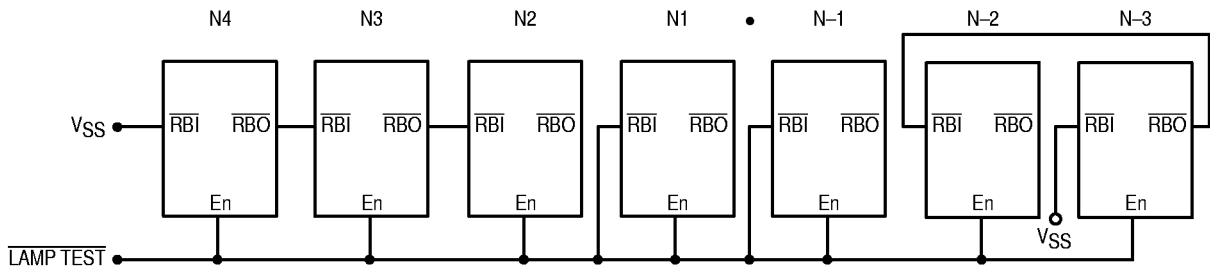


Figure 2. Leading and Trailing Zero Suppression with Lamp Test

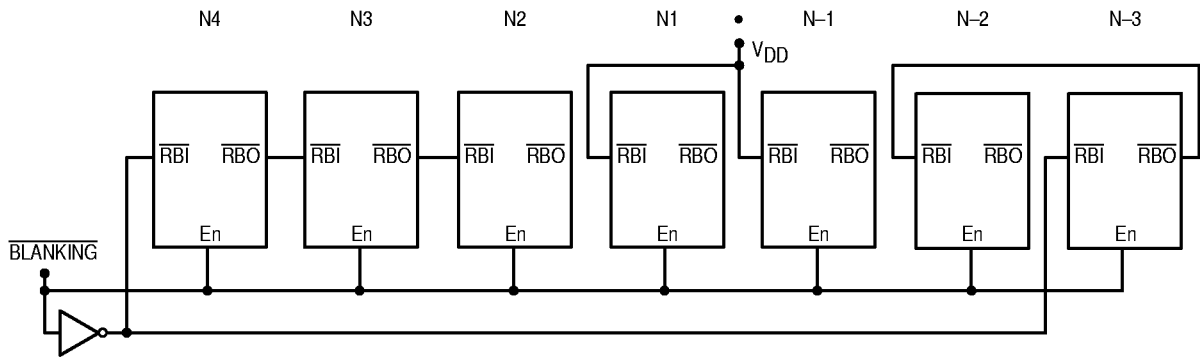


Figure 3. Leading and Trailing Zero Suppression with PWM Intensity Blanking and No Lamp Test

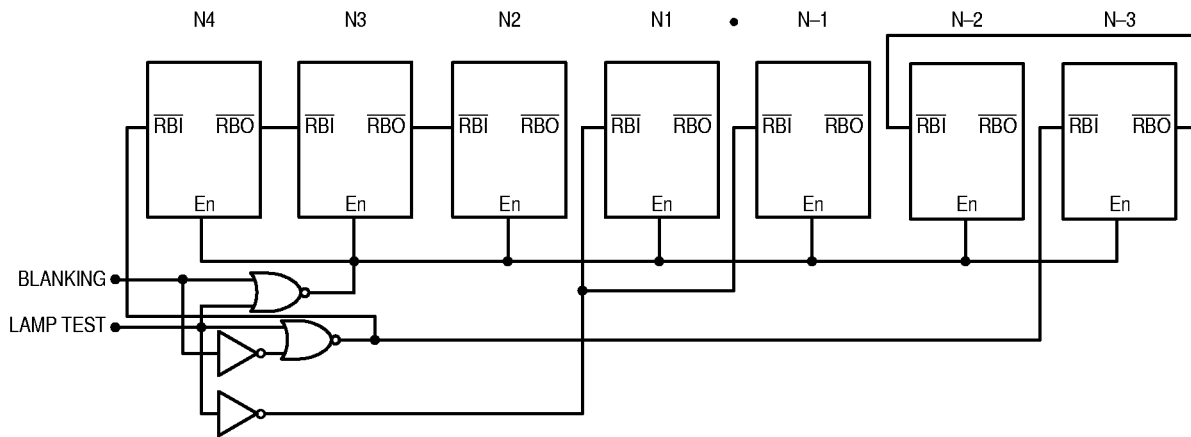
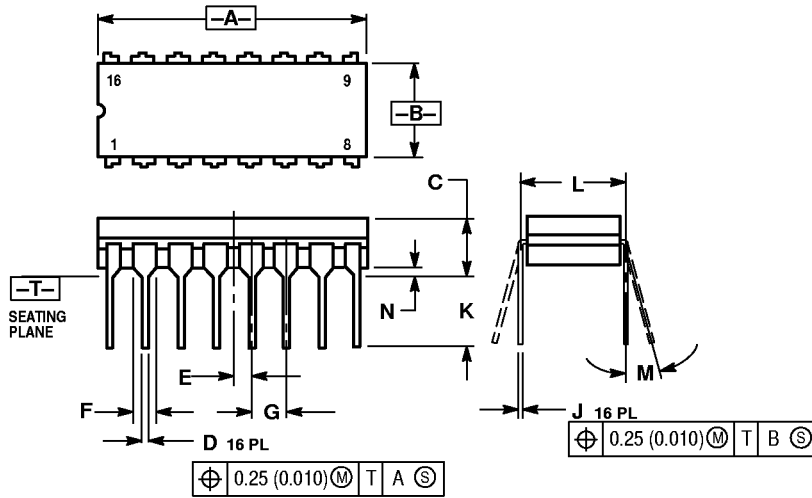


Figure 4. Zero Suppression with Lamp Test and Intensity Blanking

## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

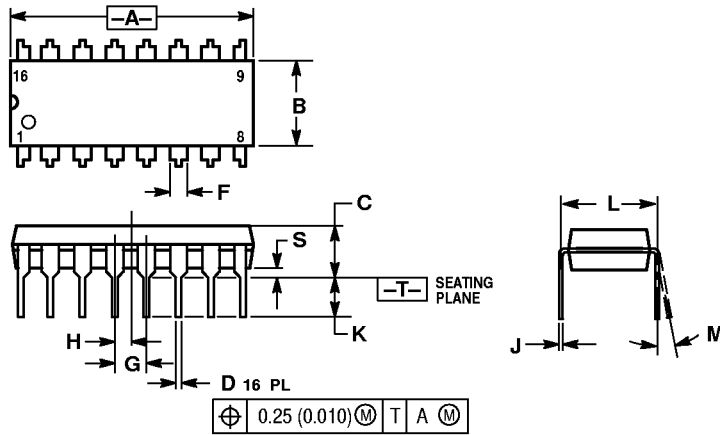


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0° 15°		0° 15°	
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



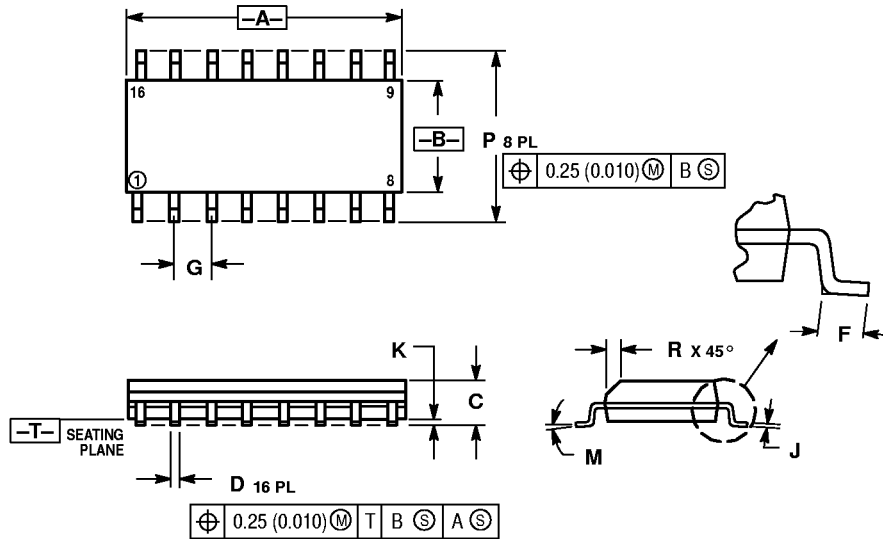
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS


### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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MC14558B/D

