TC74ACT564, 574 Octal D-Type Flip-Flop with 3-State Output

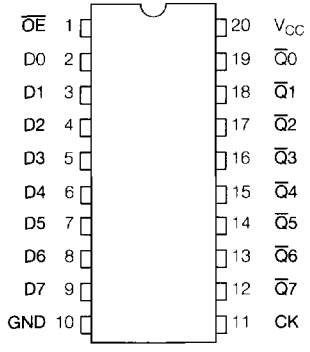
564: Inverting
574: Non-Inverting

Features:

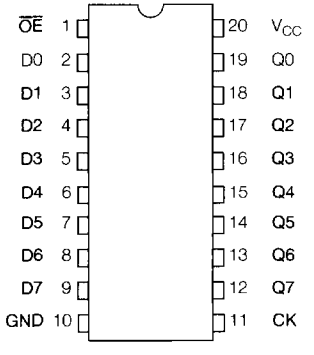
- **High Speed:** f_{MAX} = 180MHz (typ.) at V_{CC} = 5V
- **Low Power Dissipation:** I_{CC} = 8μA (max.) at Ta = 25°C
- **Compatible with TTL Outputs:** V_{IL} = 0.8V; V_{IH} = 2V (min.)
- **Symmetrical Output Impedance:** $|I_{OH}| = I_{OL}$ = 24mA (min.). Capability of driving 50Ω transmission lines.
- **Balanced Propagation Delays:** $t_{pLH} = t_{pHL}$
- **Pin and Function Compatible with 74F564/574**
- **ACT564 Available in DIP, SOIC and SOP Packages**
- **ACT574 Available in DIP, SOIC, SOP and SSOP Packages**

Pin Assignment

TC74ACT564



TC74ACT574



The TC74ACT564 and TC74ACT574 are advanced high speed CMOS OCTAL FLIP-FLOPS with 3-STATE OUTPUTS fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

These devices may be used as level converters for interfacing TTL or NMOS to high speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

These 8-bit D-type flip-flops are controlled by a latch enable input (CK) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74ACT564 is an inverting type, and the TC74ACT574 is a non-inverting type.

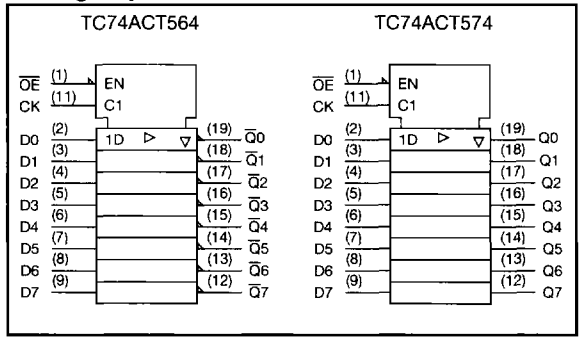
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Truth Table

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(574)	$\overline{Q}$(564)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q}_n$
L	↑	L	L	H
L	↑	H	H	L

X: Don't Care
Z: High Impedance
Q_n ($\overline{Q}_n$): No Change

IEC Logic Symbol



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP) */180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~10	ns/v

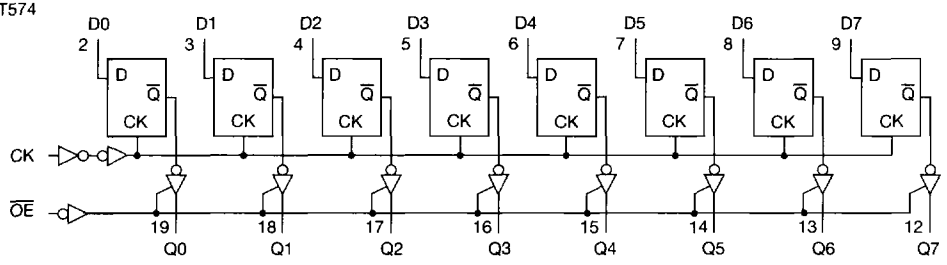
DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40~85°C Min.	Ta = -40~85°C Max.	UNIT
High-Level Input Voltage	V_{IH}			4.5~5.5	2.0	—	—	2.0	—	V
Low-Level Input Voltage	V_{IL}			4.5~5.5	—	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	
	ΔI_{CC}	Per input: V_{CC} = 3.4V Other input: V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

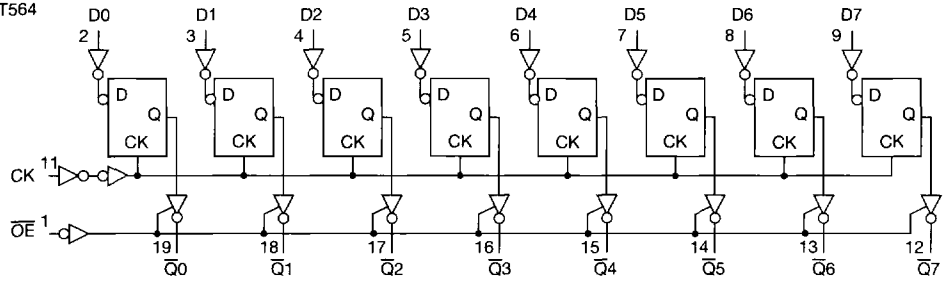
* This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.

System Diagram

TC74ACT574



TC74ACT564



Timing Requirements (Input $t_r = t_f = 3n$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C		Ta= -40~85°	UNIT
			V_{CC}	Typ.	Max.	Max.	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$	—	5.0±0.5	—	5.0	5.0	ns
Minimum Set-up Time	t_s	—	5.0±0.5	—	3.0	3.0	
Minimum Hold Time	t_h	—	5.0±0.5	—	2.0	2.0	

AC Electrical Characteristics (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Propagation Delay Time (CK–Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	5.0±0.5	—	6.2	10.1	1.0	11.5	ns
Output Enable Time	t_{pZL} t_{pZH}	—	5.0±0.5	—	6.3	10.5	1.0	12.0	
Output Disable Time	t_{pLZ} t_{pHZ}	—	5.0±0.5	—	6.6	9.6	1.0	11.0	
Maximum Clock Frequency	f_{MAX}	—	5.0±0.5	85	160	—	85	—	MHz
Input Capacitance	C_{IN}	—	—	—	5	10	—	10	pF
Output Capacitance	C_{OUT}	—	—	—	10	—	—	—	
Power Dissipation Capacitance	C_{PD} (1)	—	—	—	33	—	—	—	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC\ (opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC} / 8$ (per F/F). And the total C_{PD} when n pcs. of Flip-Flop operate can be gained by the following equation: C_{PD} (total)=21+12 • n.