

DATA SHEET

74ALVT16373

**2.5V/3.3V 16-bit transparent
D-type latch (3-State)**

Product specification
Supersedes data of 1996 May 29
IC23 Data Handbook

1998 Feb 13

2.5V/3.3V 16-bit transparent D-type latch (3-State)**74ALVT16373****FEATURES**

- 16-bit transparent latch
- 5V I/O compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16373 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When latch enable (LE) input is High, the Q outputs follow the data (D) inputs. When latch enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	$C_L = 50\text{pF}$	2.0 2.4	1.6 1.8	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or 3.0V	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

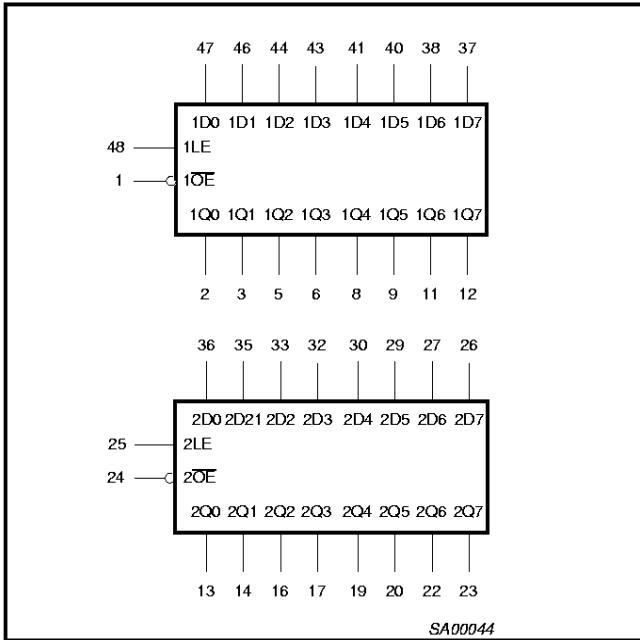
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ALVT16373 DL	AV16373 DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ALVT16373 DGG	AV16373 DGG	SOT362-1

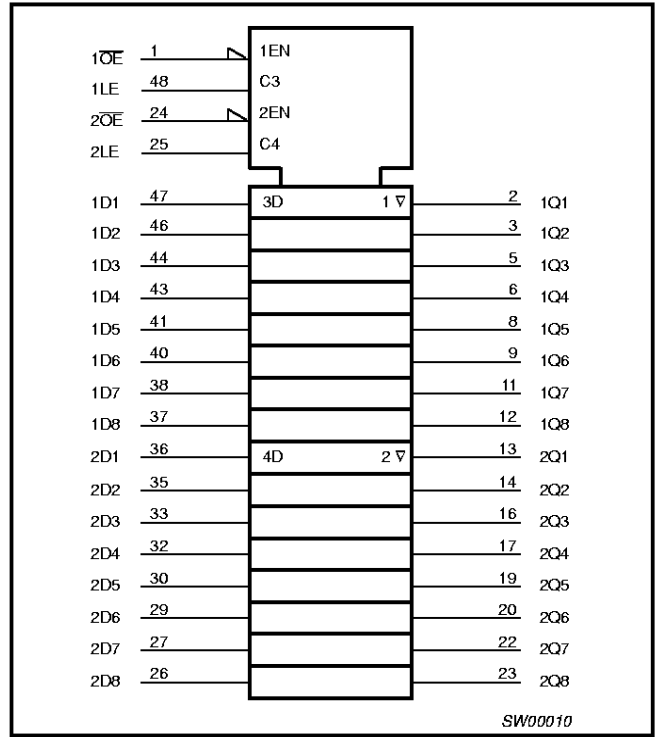
2.5V/3.3V 16-bit transparent D-type latch (3-State)

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LOGIC SYMBOL



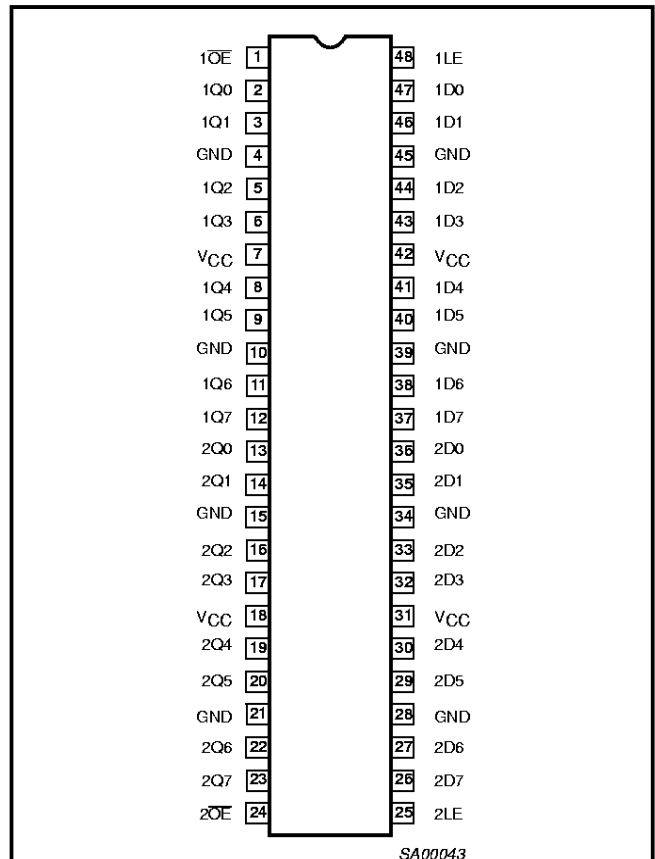
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$\overline{1OE}$, $\overline{2OE}$	Output enable inputs (active-Low)
48, 25	1LE, 2LE	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage

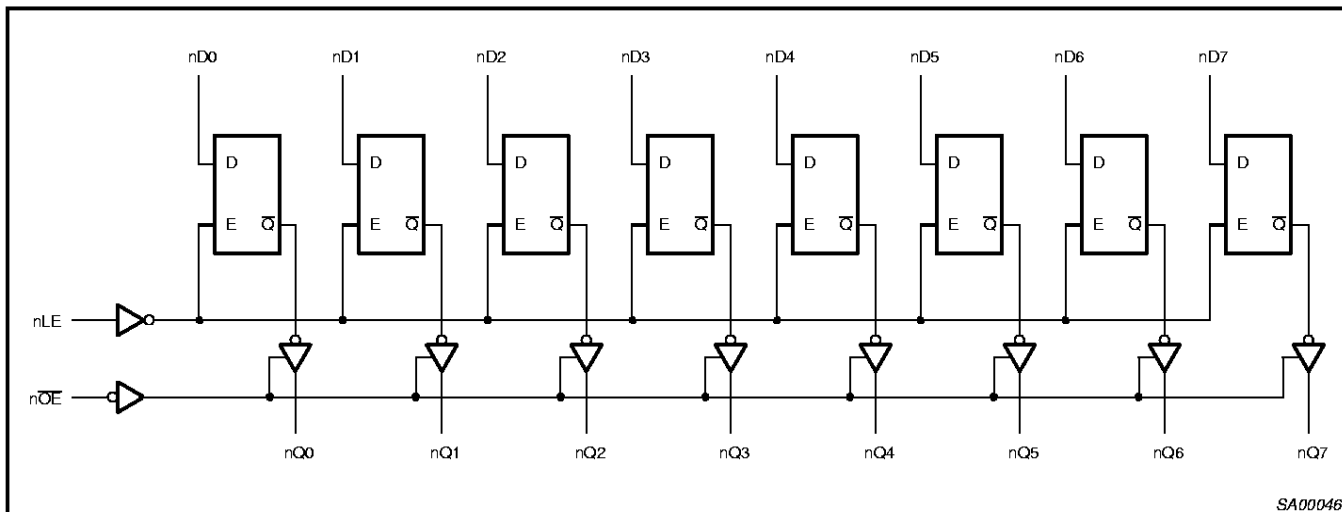
PIN CONFIGURATION



2.5V/3.3V 16-bit transparent D-type latch (3-State)

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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS nQ0 – nQ7	OPERATING MODE
nOE	nE	nDx			
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	nDx	nDx	Z	

H = High voltage level
 h = High voltage level one set-up time prior to the High-to-Low E transition
 L = Low voltage level
 l = Low voltage level one set-up time prior to the High-to-Low E transition
 NC= No change
 X = Don't care
 Z = High impedance "off" state
 ↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage ³		-0.5 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V _I	Input voltage	0	5.5	0	5.5	V
V _{IH}	High-level input voltage	1.7		2.0		V
V _{IL}	Input voltage		0.7		0.8	V
I _{OH}	High-level output current		-8		-32	mA
I _{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 3.0V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 3.0 to 3.6V; I _{OH} = -100μA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 3.0V; I _{OH} = -32mA	2.0	2.3		
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 100μA		0.07	0.2	V
		V _{CC} = 3.0V; I _{OL} = 16mA		0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA		0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA		0.4	0.55	
V _{RST}	Power-up output low voltage ⁶	V _{CC} = 3.6V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins	0.1	±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V		0.1	10	
		V _{CC} = 3.6V; V _I = V _{CC}	Data pins ⁴	0.5	1	
		V _{CC} = 3.6V; V _I = 0V		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	μA
I _{HOLD}	Bus Hold current Data inputs ⁷	V _{CC} = 3V; V _I = 0.8V	75	130		μA
		V _{CC} = 3V; V _I = 2.0V	-75	-140		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V	±500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V		10	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care		1	±100	μA
I _{OZH}	3-State output High current	V _{CC} = 3.6V; V _O = 3.0V; V _I = V _{IL} or V _{IH}		0.5	5	μA
I _{OZL}	3-State output Low current	V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		0.5	-5	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.04	0.1	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		3.5	5	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.05	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

2.5V/3.3V 16-bit transparent D-type latch (3-State)

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AC CHARACTERISTICS (3.3V ± 0.3V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$			
			MIN	TYP ¹	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	0.5 0.5	1.6 1.8	2.5 2.9	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.0 1.0	2.0 2.3	3.1 3.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.5 1.0	2.3 1.9	4.0 3.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5	1.5 1.5	2.9 2.3	4.5 3.7	ns

NOTE:1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.**DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)**

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to $+85^\circ\text{C}$			
			MIN	TYP ¹	MAX	
V_{IK}	Input clamp voltage	$V_{CC} = 2.3V$; $I_{IK} = -18\text{mA}$		-0.85	-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = 2.3$ to $3.6V$; $I_{OH} = -100\mu\text{A}$ $V_{CC} = 2.3V$; $I_{OH} = -8\text{mA}$	$V_{CC}-0.2$ 1.8			V
V_{OL}	Low-level output voltage	$V_{CC} = 2.3V$; $I_{OL} = 100\mu\text{A}$ $V_{CC} = 2.3V$; $I_{OL} = 24\text{mA}$		0.07 0.3	0.2 0.5	
V_{RST}	Power-up output low voltage ⁷	$V_{CC} = 2.7V$; $I_O = 1\text{mA}$; $V_I = V_{CC}$ or GND			0.55	V
I_I	Input leakage current	$V_{CC} = 2.7V$; $V_I = V_{CC}$ or GND	Control pins	0.1	±1	μA
		$V_{CC} = 0$ or $2.7V$; $V_I = 5.5V$		0.1	10	
		$V_{CC} = 2.7V$; $V_I = V_{CC}$	Data pins ⁴	0.1	1	
		$V_{CC} = 2.7V$; $V_I = 0$		0.1	-5	
I_{OFF}	Off current	$V_{CC} = 0V$; V_I or $V_O = 0$ to $4.5V$		0.1	±100	μA
I_{HOLD}	Bus Hold current	$V_{CC} = 2.3V$; $V_I = 0.7V$		90		μA
	Data inputs ⁶	$V_{CC} = 2.3V$; $V_I = 1.7V$		-10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	$V_O = 5.5V$; $V_{CC} = 2.3V$		10	125	μA
$I_{PU/PD}$	Power up/down 3-State output current ³	$V_{CC} \leq 1.2V$; $V_O = 0.5V$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; OE/OE = Don't care		1	100	μA
I_{OZH}	3-State output High current	$V_{CC} = 2.7V$; $V_O = 2.3V$; $V_I = V_{IL}$ or V_{IH}		0.5	5	μA
I_{OZL}	3-State output Low current	$V_{CC} = 2.7V$; $V_O = 0.5V$; $V_I = V_{IL}$ or V_{IH}		0.5	-5	μA
I_{CCH}	Quiescent supply current	$V_{CC} = 2.7V$; Outputs High, $V_I = \text{GND}$ or V_{CC} , $I_O = 0$		0.04	0.1	mA
I_{CCL}		$V_{CC} = 2.7V$; Outputs Low, $V_I = \text{GND}$ or V_{CC} , $I_O = 0$		2.3	4.5	
I_{CCZ}		$V_{CC} = 2.7V$; Outputs Disabled; $V_I = \text{GND}$ or V_{CC} , $I_O = 0^5$		0.04	0.1	
ΔI_{CC}	Additional supply current per input pin ²	$V_{CC} = 2.3V$ to $2.7V$; One input at $V_{CC}-0.6V$, Other inputs at V_{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at $V_{CC} = 2.5V$ and $T_{\text{amb}} = 25^\circ\text{C}$.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From $V_{CC} = 1.2V$ to $V_{CC} = 2.5V \pm 0.2V$ a transition time of 100 μsec is permitted. This parameter is valid for $T_{\text{amb}} = 25^\circ\text{C}$ only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- Not guaranteed.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

2.5V/3.3V 16-bit transparent D-type latch (3-State)

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AC CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5V \pm 0.2V$			
			MIN	TYP ¹	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.0 1.0	2.0 2.4	3.2 4.2	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.5 1.5	2.6 2.8	4.2 4.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	2.0 1.5	3.5 2.6	5.5 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5	1.5 1.0	2.7 2.0	4.5 3.5	ns

NOTE:

1. All typical values are at $V_{CC} = 2.5V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 3.3V \pm 0.3V$		
			MIN	TYP	MIN	TYP	
$t_S(H)$ $t_S(L)$	Setup time nDx to nE	3	0 1.5	-0.7 0.2	0.5 0.8	-0.2 0.2	ns
$t_H(H)$ $t_H(L)$	Hold time nDx to nE	3	0.5 1.5	-0.2 0.7	0.8 1.0	0 0.2	ns
$t_W(H)$	nE pulse width High	1	1.5 1.5		1.5 1.5		ns

AC WAVEFORMS

For all waveforms

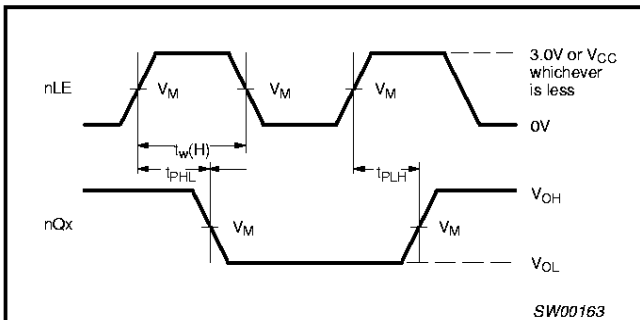
$V_M = 1.5V$ for $V_{CC} \geq 3.0V$; $V_M = V_{CC}/2$ for $V_{CC} \leq 2.7V$

$V_M = 1.5V$ for $V_{CC} \geq 3.0V$; $V_M = V_{CC}/2$ for $V_{CC} \leq 2.7V$

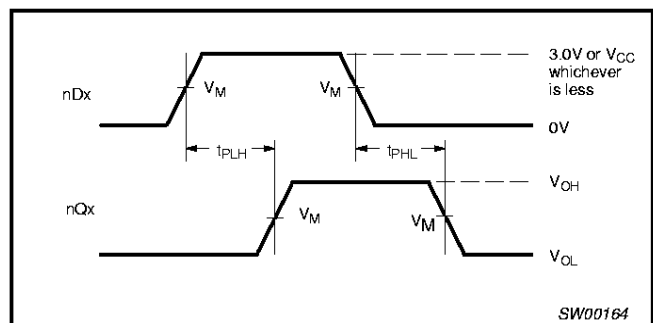
$V_X = V_{OL} + 0.3V$ for $V_{CC} \geq 3.0V$; $V_X = V_{OL} + 0.15V$ for $V_{CC} \leq 2.7V$

$V_Y = V_{OH} - 0.3V$ for $V_{CC} \geq 3.0V$; $V_Y = V_{OH} - 0.15V$ for $V_{CC} \leq 2.7V$

2.7V



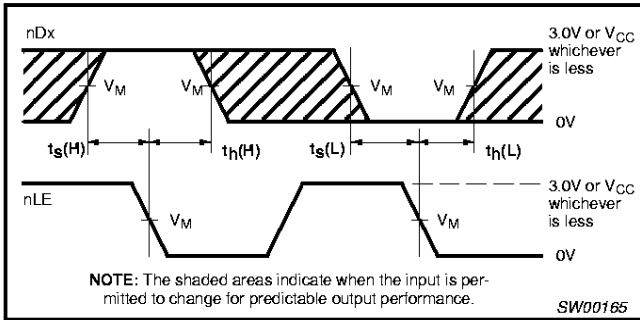
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



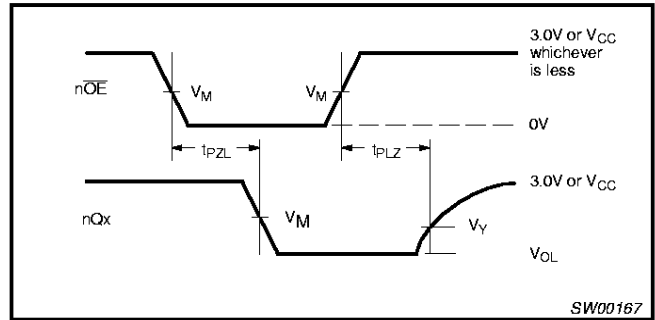
Waveform 2. Propagation Delay for Data to Outputs

2.5V/3.3V 16-bit transparent D-type latch (3-State)

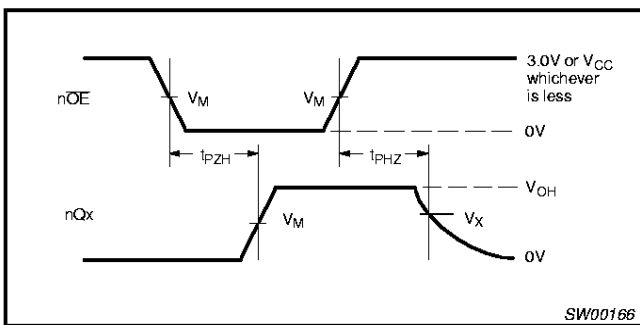
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Waveform 3. Data Setup and Hold Times



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 4. 3-State Output Enable time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION	
TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or $V_{CC} \times 2$
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

$V_M = 1.5V \text{ or } V_{CC} / 2, \text{ whichever is less}$

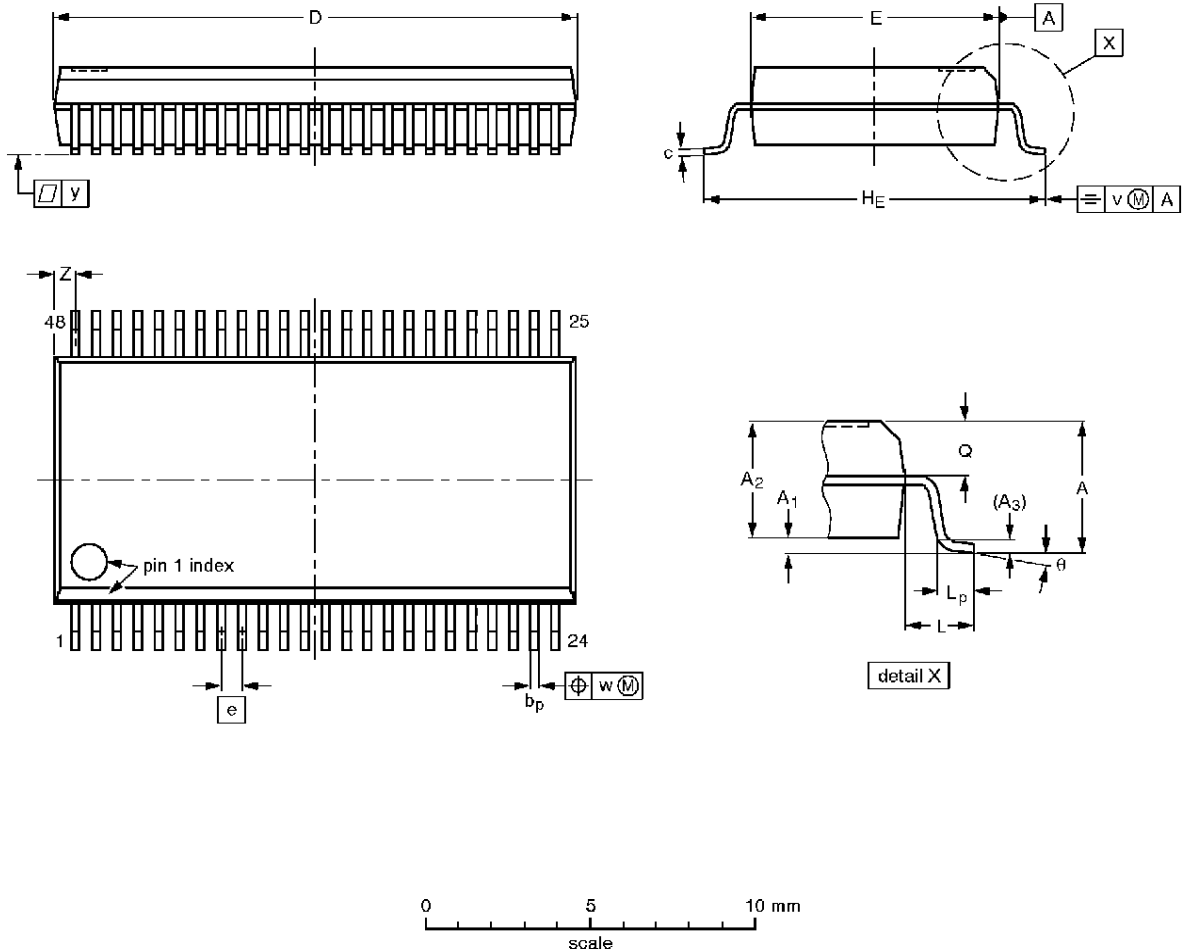
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

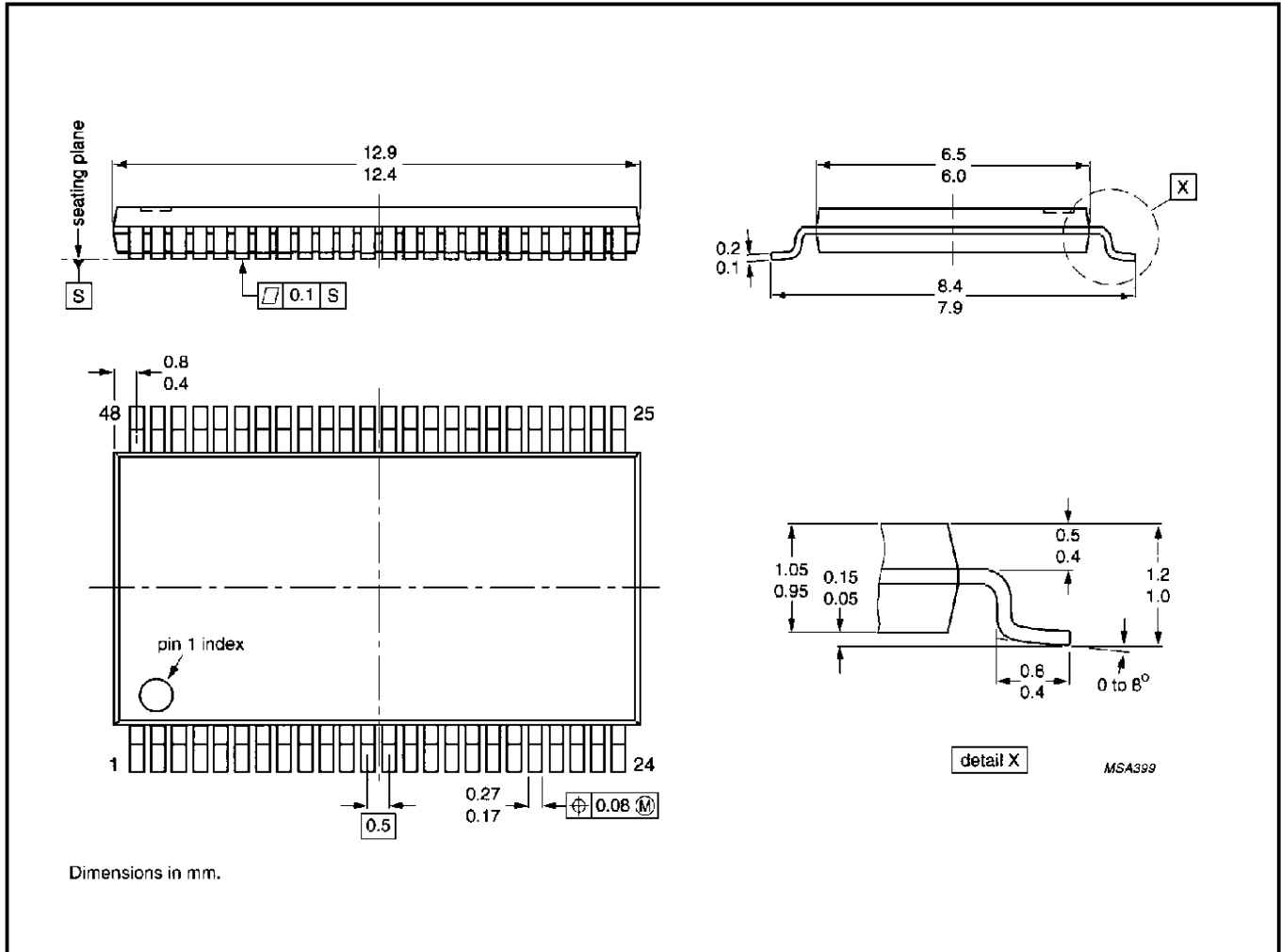
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02 95-02-04

2.5V/3.3V 16-bit transparent D-type latch (3-State)

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



2.5V/3.3V 16-bit transparent D-type latch (3-State)

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NOTES

2.5V/3.3V 16-bit transparent D-type latch (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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