

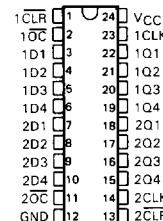
**SN54ALS878A, SN54ALS879A, SN54AS878, SN54AS879
SN74ALS878A, SN74ALS879A, SN74AS878, SN74AS879**
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661 APRIL 1982 REVISED MAY 1986

- 3-State Bus Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Choice of True or Inverting Logic
 'ALS878A, 'AS878 True Outputs
 'ALS879A, 'AS879 Inverting Outputs
- Synchronous Clear
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

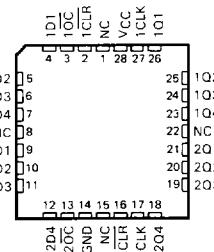
SN54ALS878A, SN54AS878 . . . JT PACKAGE
SN74ALS878A, SN74AS878 . . . DW OR NT PACKAGE

(TOP VIEW)



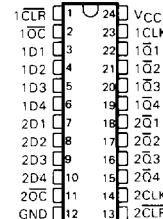
SN54ALS878A, SN54AS878 . . . FK PACKAGE
SN74ALS878A, SN74AS878 . . . FN PACKAGE

(TOP VIEW)



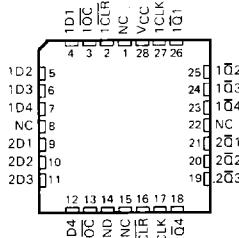
SN54ALS879A, SN54AS879 . . . JT PACKAGE
SN74ALS879A, SN74AS879 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54ALS879A, SN54AS879 . . . FK PACKAGE
SN74ALS879A, SN74AS879 . . . FN PACKAGE

(TOP VIEW)



NC No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**SN54ALS878A, SN54ALS879A, SN54AS878, SN54AS879
SN74ALS878A, SN74ALS879A, SN74AS878, SN74AS879
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

'ALS878A, 'AS878
(EACH FLIP-FLOP)

INPUTS			OUTPUT	
OC	CLR	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q ₀
H	X	X	X	Z

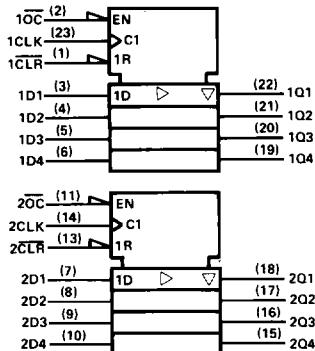
FUNCTION TABLES

'ALS879A, 'AS879
(EACH FLIP-FLOP)

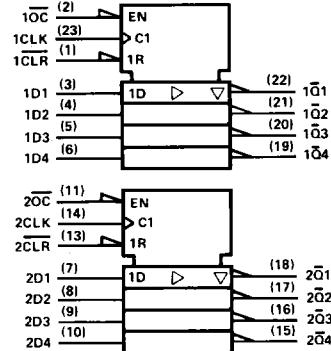
INPUTS			OUTPUT	
OC	CLR	CLK	D	Q̄
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	Q ₀
H	X	X	X	Z

logic symbols †

'ALS878A, 'AS878

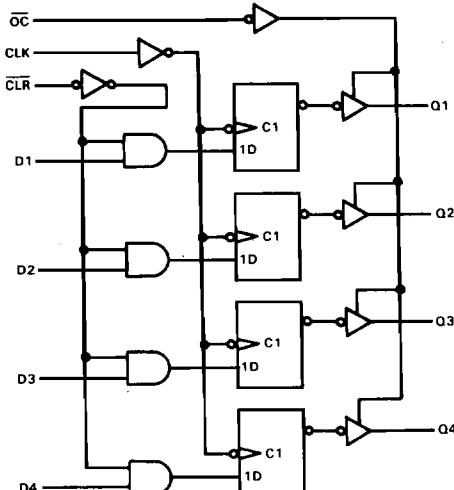


'ALS879A, 'AS879

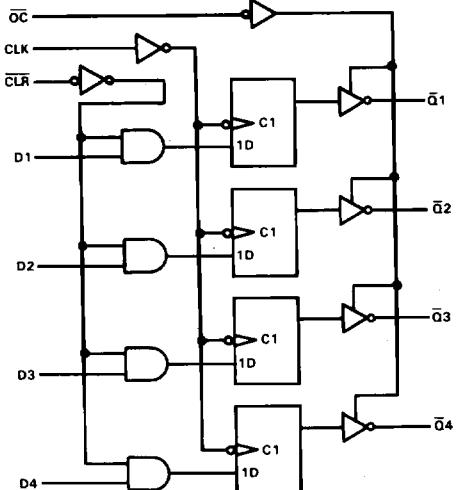


logic diagrams (positive logic)

'ALS878A, AS878 (EACH QUAD FLIP-FLOP)



'ALS879A, 'AS879 (EACH QUAD FLIP-FLOP)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

SN54ALS878A, SN54ALS879A, SN74ALS878A, SN74ALS879A

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS878A, SN54ALS879A	-55°C to 125°C
SN74ALS878A, SN74ALS879A	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS878A SN54ALS879A			SN74ALS878A SN74ALS879A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2	2	V
V _{IL}	Low-level input voltage	0.7	0.8	V
I _{OH}	High-level output current	-1	-2.6	mA
I _{OL}	Low-level output current	12	24	mA
f _{clock}	Clock frequency	'ALS878A	0	25	0	30	MHz
		'ALS879A	0	20	0	25	
t _w	Pulse duration	'ALS878A CLK high or low	20	16.5	ns
		'ALS879A CLK high or low	25	20	
t _{su}	Setup time before CLK1	Data	15	15	ns
		CLR	20	20	
t _h	Hold time after CLK1	Data	4	4	ns
		CLR	0	0	
T _A	Operating free-air temperature	-55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS878A SN54ALS879A			SN74ALS878A SN74ALS879A			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2	-1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} 2	V _{CC} 2	V
	V _{CC} = 4.5 V, I _{OH} = 1 mA	2.4	3.3	
	V _{CC} = 4.5 V, I _{OH} = -2.6 mA	2.4	3.2	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V
	V _{CC} = 4.5 V, I _{OL} = 24 mA	0.35	0.5	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	20	20	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	-20	-20	μA
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1	0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20	20	μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	-0.2	-0.2	mA
I _{O[‡]}	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	-30	-112	mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	14	23	14	23	mA
		Outputs low	18	31	18	31	
		Outputs disabled	20	33	20	33	

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS878A, SN54ALS879A, SN74ALS878A, SN74ALS879A DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT		
			'ALS878A 'ALS879A			SN54ALS878A SN54ALS879A	SN74ALS878A SN74ALS879A		
			MIN	TYP	MAX	MIN	MAX		
f _{max}	'ALS878A		40	50	25	30		MHz	
	'ALS879A		40	50	20	25			
t _{PLH}	CLK	Q or \bar{Q}	8	10	4	15	4	14	
t _{PHL}			9	13	4	17	4	16	
t _{PZH}	\overline{OC}	Q or \bar{Q}	9	13	4	22	4	20	
t _{PZL}			11	15	4	22	4	20	
t _{PHZ}	\overline{OC}	Q or \bar{Q}	6	8	2	12	2	10	
t _{PLZ}			7	10	3	18	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS878, SN54AS879, SN74AS878, SN74AS879
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V		
Input voltage	7 V		
Voltage applied to a disabled 3-state output	5.5 V		
Operating free-air temperature range SN54AS878, SN54AS879	−55 °C to 125 °C		
SN74AS878, SN74AS879	0 °C to 70 °C		
Storage temperature range	−65 °C to 150 °C		

recommended operating conditions

		SN54AS878			SN74AS878			UNIT	
		SN54AS879			SN74AS879				
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V _{IH}	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage			0.8			0.8	V	
I _{OH}	High-level output current			−12			−15	mA	
I _{OL}	Low-level output current			32			48	mA	
f _{clock}	Clock frequency	0	100		0	125		MHz	
t _w	Pulse duration	CLK low	4		2			ns	
		CLK high	5		4				
t _{su}	Setup time	Data	3		2			ns	
	before CLK!	CLR	6.5		5.5				
t _h	Hold time	Data	3		2			ns	
	after CLK!	CLR	0		0				
T _A	Operating free-air temperature	−55		125	0	70		°C	

SN54AS878, SN54AS879, SN74AS878, SN74AS879

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS878 SN54AS879			SN74AS878 SN74AS879			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-	-1.2	-	-	-1.2	-	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2	-	-	V _{CC} -2	-	-	V
	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.2	-	-	-	-	
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 32 mA	-	0.29	0.5	-	0.33	0.5	V
	V _{CC} = 4.5 V, I _{OL} = 48 mA	-	-	-	-	-	-	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	-	-	50	-	-	50	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	-	-	-50	-	-	-50	μA
I _I	V _{CC} = 5.5 V, V _I = 7 V	-	-	0.1	-	-	0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	-	-	20	-	-	20	μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	-	-	-3	-	-	-2	mA
	All other	-	-	-0.5	-	-	-0.5	
I _O [‡]	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112	-30	-112	mA
I _{CC}	AS878 See Note 1	Outputs high	82	132	82	132	-	mA
		Outputs low	96	155	96	155	-	
		Outputs disabled	100	160	100	160	-	
		Outputs high	88	142	88	142	-	
		Outputs low	94	150	94	150	-	
		Outputs disabled	100	160	100	160	-	

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLR and all D inputs grounded, and CLK and OC at 4.5 V.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT	
			SN54AS878 SN54AS879		SN74AS878 SN74AS879			
			MIN	MAX	MIN	MAX		
f _{max}	-	-	100	-	125	-	MHz	
t _{PLH}	CLK	Q or \bar{Q}	3	11.5	3	8.5	ns	
t _{PHL}			4	12.5	4	10.5		
t _{PZH}	\bar{OC}	Q or \bar{Q}	2	8	2	7	ns	
t _{PZL}			3	11.5	3	10.5		
t _{PHZ}	\bar{OC}	Q or \bar{Q}	2	7	2	6	ns	
t _{PLZ}			2	7	2	6		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.