

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **Typical $t_{sk(o)}$ (Output Skew) < 250ps**
 - ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
 - 25 mil pitch SSOP, 19.6 mil pitch TSSOP,
and 15.7 mil pitch TVSOP packages
 - Extended commercial range of -40°C to +85°C
 - $V_{CC} = 3.3V \pm 0.3V$, Normal Range
 - $V_{CC} = 2.7V$ to $3.6V$, Extended Range
 - $V_{CC} = 2.5V \pm 0.2V$
 - CMOS power levels (0.4 μ W typ. static)
 - Rail-to-Rail output swing for increased noise margin
- **Features for ALVCH16244 and ALVC16244:**
 - High Drive Outputs: $\pm 24mA$
 - Suitable for heavy loads
- **Features for ALVCH162244 and ALVC162244:**
 - Light Balanced Output Driver: $\pm 12mA$
 - Minimal switching noise

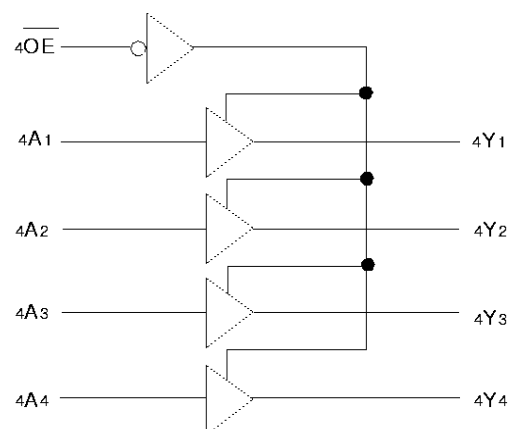
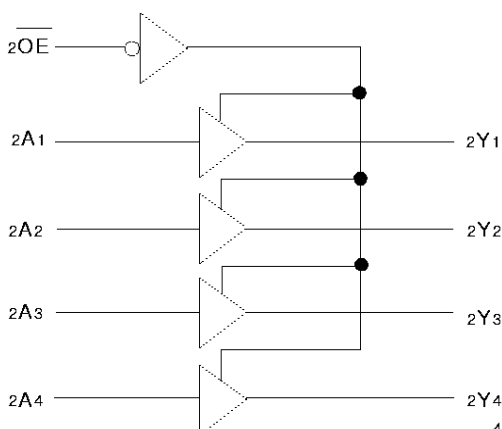
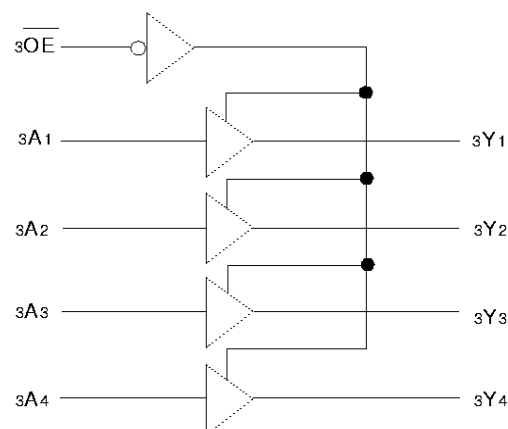
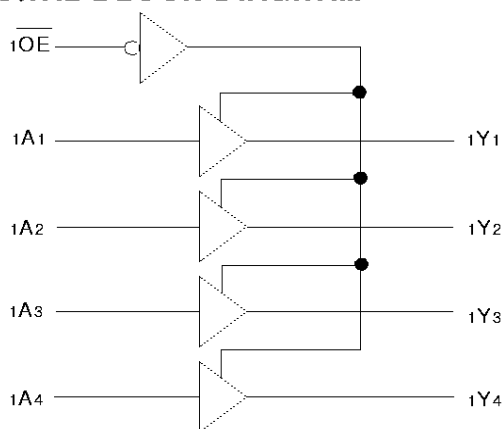
DESCRIPTION:

The 16-bit buffer line drivers are built using advanced dual metal CMOS technology. These high-speed, low power devices offer bus/backplane interface capability with improved packing density and a flow-through organization for simplifying board layout. The three-state controls operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

The ALVCH16x244 have "bus-hold" which retains the input's last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

The ALVCH16244/ALVC16244 have been designed with a $\pm 24mA$ output driver. These drivers are capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH162244/ALVC162244 have series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12mA$ at the designated threshold levels.

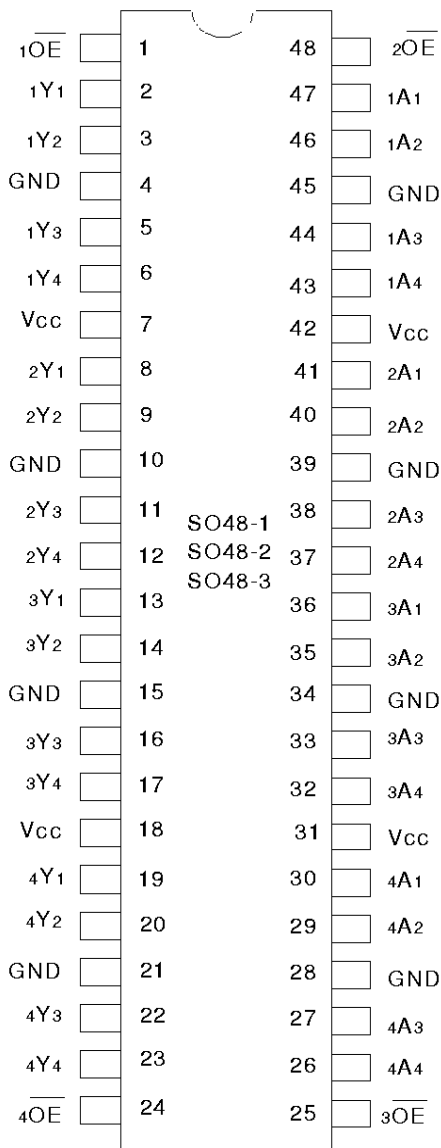
FUNCTIONAL BLOCK DIAGRAM


4210 drw 01

4210 drw 02

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PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

4210 dnw 03

ABSOLUTE MAXIMUM RATING⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +60	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	-50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
\overline{xOE}	xAx	xYx
L	L	L
L	H	H
H	X	Z

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NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

PIN DESCRIPTION

Pin Names	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Data Inputs ⁽¹⁾
xYx	3-State Outputs

NOTE:

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- On ALVCH these pins have "Bus-hold". All other pins are standard inputs, outputs or I/Os. On ALVC no pins have "Bus-hold".

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5.0	7.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7.0	9.0	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7.0	9.0	pF

NOTE:

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- As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	Vcc = 2.3V to 2.7V		1.7	—	—	V
		Vcc = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	Vcc = 2.3V to 2.7 V		—	—	0.7	V
		Vcc = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	Vcc = 3.6V	Vi = Vcc	—	—	±1	µA
IiL	Input LOW Current	Vcc = 3.6V	Vi = GND	—	—	±1	
IoZH IoZL	High Impedance Output Current (3-State Output pins)	Vcc = 3.6V	Vo = Vcc	—	—	±1	µA
			Vo = GND	—	—	±1	
VIK	Clamp Diode Voltage	Vcc = 2.3V, IIN = -18mA		—	0.7	-1.2	V
VH	Input Hysteresis	Vcc = 3.3V		—	100	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	Vcc = 3.6V VIN = GND or Vcc		—	0.1	40	µA

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BUS-HOLD CHARACTERISTICS FOR ALVCH16x244

Symbol	Parameter ⁽²⁾	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	Vcc = 3.0V	Vi = 2.0V	-75	—	—	µA
			Vi = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	Vcc = 2.3V	Vi = 1.7V	-45	—	—	µA
			Vi = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	Vcc = 3.6V	Vi = 0 to 3.6V	—	—	±500	µA

NOTES:

1. Typical values are at Vcc = 3.3V, +25°C ambient.
2. Pins with Bus-hold are identified in the pin description.

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OUTPUT DRIVE CHARACTERISTICS FOR ALVCH16244 AND ALVC16244

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} -0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = -24mA	2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

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OUTPUT DRIVE CHARACTERISTICS FOR ALVCH162244 AND ALVC162244

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} -0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -4mA	1.9	—	
		V _{CC} = 2.3V	I _{OH} = -6mA	1.7	—	
		V _{CC} = 2.7V	I _{OH} = -8mA	2	—	
		V _{CC} = 3.0V	I _{OH} = -6mA	2.4	—	
		V _{CC} = 3.0V	I _{OH} = -12mA	2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 6mA	—	0.55	
		V _{CC} = 2.7V	I _{OL} = 8mA	—	0.6	
		V _{CC} = 3.0V	I _{OL} = 12mA	—	0.8	

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NOTE:
 1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Standard Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2.0	10	μA
ΔI_{CC}	Quiescent Power Supply Current TTL Bus-Hold Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	162	325	μA
I_{CCD}	Dynamic Power Supply Current ^(4,5)	$V_{CC} = \text{Max.}$ Outputs Open 50% Duty Cycle $\overline{xOE} = \text{GND}$ One Input Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	47	60	μA / MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.47	0.64	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.55	0.8	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.9	2.4	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	3.2	5.0	

NOTES:

- $V_{CC} (\text{max.}) = 3.6V$
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- $CPD = I_{CCD}/V_{CC}$
CPD = Power Dissipation Capacitance
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

4210 tbl 09

SWITCHING CHARACTERISTICS FOR ALVCH16244 AND ALVC16244⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ±0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay xAx to xYx	1	4.3	1	3.6	1	3.0	ns
tpZH tpZL	Output Enable Time	1	6.2	1	5.4	1	4.4	ns
tpHZ tplZ	Output Disable Time	1	5.4	1	4.6	1	4.1	ns
tsk(o)	Output Skew ⁽²⁾	0	500	0	500	0	500	ps

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SWITCHING CHARACTERISTICS FOR ALVCH162244 AND ALVC162244⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ±0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay xAx to xYx	1	5.0	1	4.0	1	3.6	ns
tpZH tpZL	Output Enable Time	1	6.8	1	6.0	1	5.0	ns
tpHZ tplZ	Output Disable Time	1	6.0	1	5.2	1	5.0	ns
tsk(o)	Output Skew ⁽²⁾	0	500	0	500	0	500	ps

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NOTES:

1. See test circuits and waveforms. T_A = -40°C to +85°C.
2. Skew between any two outputs of the same package switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

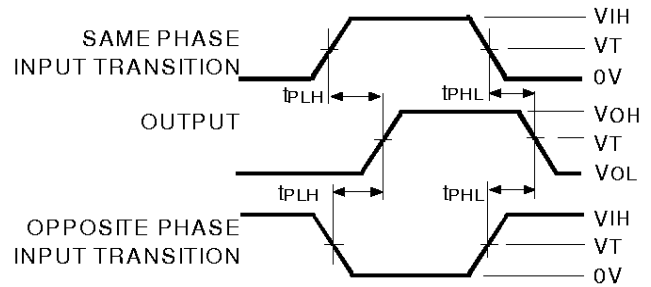
Symbol	V _{CC} = 3.3V ±0.3V	V _{CC} = 2.7V	V _{CC} = 2.5V ±0.2V	Unit
V _{LOAD}	6	6	4.6	V
V _{IH}	2.7	2.7	2.3	V
V _T	1.5	1.5	V _{CC} /2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

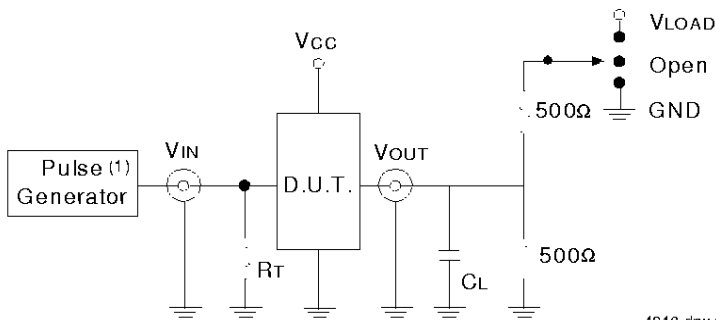
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PROPAGATION DELAY



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TEST CIRCUITS FOR ALL OUTPUTS

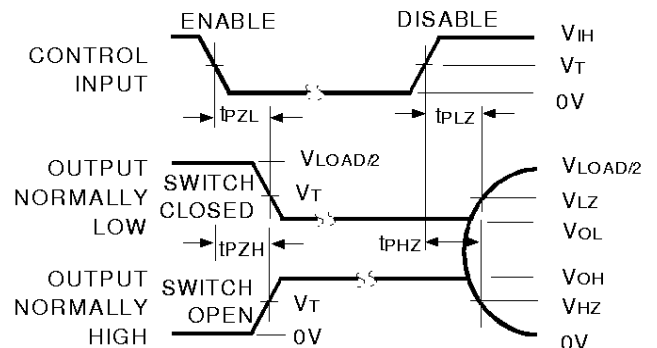


4210 drw 04

NOTE:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ENABLE AND DISABLE TIMES



NOTE:

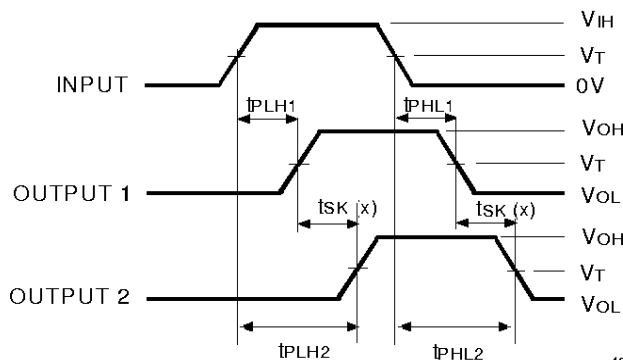
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

4210 drw 08

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

OUTPUT SKEW - t_{SK} (x)



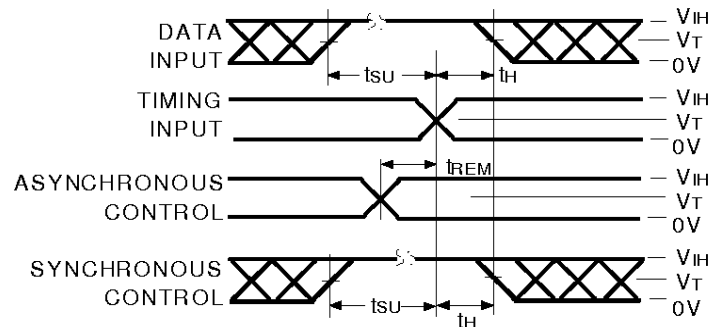
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$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

NOTES:

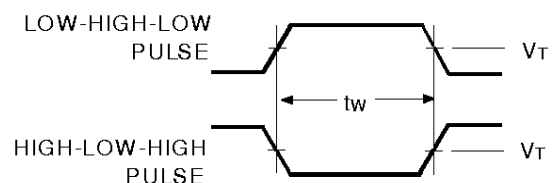
1. For t_{SK(o)} OUTPUT1 and OUTPUT2 are any two outputs.
 2. For t_{SK(b)} OUTPUT1 and OUTPUT2 are in the same bank.

SET-UP, HOLD AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
Temp. Range	Bus-Hold	Family	Device Type	Package			
						PV	Shrink Small Outline Package (SO48-1)
						PA	Thin Shrink Small Outline Package (SO48-2)
						PF	Thin Very Small Outline Package (SO48-3)
					244		16-Bit Buffer/Line Driver
					16		Double-Density 3.3Volt w/Resistors, ±24mA
					162		Double-Density 3.3Volt w/Resistors, ±12mA
					Blank		No-Bus-hold
					H		Bus-hold
					74		-40°C to +85°C

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