MOTOROLA

Quad 2-Input NAND Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/33001

Military 54F00

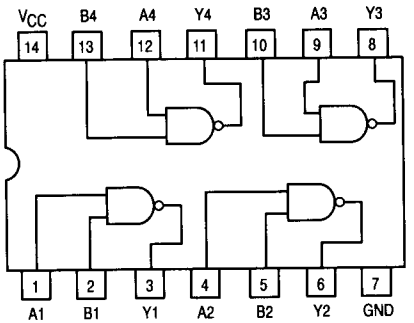
AVAILABLE AS:

1) JAN: JM38510/33001BXA
2) SMD: N/A
3) 883: 54F00/BXAJC

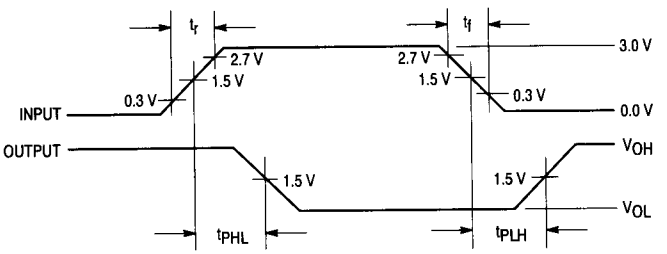
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

LOGIC DIAGRAM

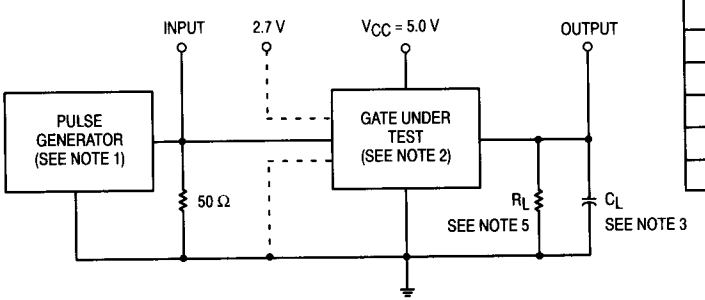


WAVEFORMS



NOTES:
1. Pulse generator has the following characteristics: $t_r = t_f = 6.0 \pm 1.5$ ns, PRR = 1.0 MHz, and $Z_{OUT} \approx 50\ \Omega$.
2. Terminal condition (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_L = 500\ \Omega \pm 5.0\%$.

AC TEST CIRCUIT



PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	V_{CC}
B1	2	2	3	V_{CC}
Y1	3	3	4	OPEN
A2	4	4	6	V_{CC}
B2	5	5	8	V_{CC}
Y2	6	6	9	OPEN
GND	7	7	10	GND
Y3	8	8	12	OPEN
A3	9	9	13	V_{CC}
B3	10	10	14	V_{CC}
Y4	11	11	16	OPEN
A4	12	12	18	V_{CC}
B4	13	13	19	V_{CC}
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IL} = 0.8 V, V_{IN} = 5.5 V on other input.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IH} = 2.0 V on both inputs.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other input is open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IN} = 2.7 V, other input = 0 V.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IN} = 7.0 V, other input = 0 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs = 5.5 V.
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 4.5 V, both inputs = 5.5 V, V_{OUT} = 2.5 V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), V_{OUT} = 0 V.
I_{CCH}	Power Supply Current		2.8		2.8		2.8	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCL}	Power Supply Current		10.2		10.2		10.2	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay /Data-Output Output High-Low	1.5	4.3	1.5	6.5	1.5	6.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH}	Propagation Delay /Data-Output Output Low-High	2.4	5.0	2.0	7.0	2.0	7.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.