

LF155/156/157 JFET-Input Operational Amplifiers

Features

All Devices

- Low input offset voltage — 0.3 mV
- High common mode rejection ratio — 100 dB
- Low input bias current — 30 pA
- Low input noise current — $0.01 \text{ pA}/\sqrt{\text{Hz}}$
- Low input offset voltage drift — $3.0 \text{ } \mu\text{V}/^\circ\text{C}$

LF155 Only

- Low supply current — 2.5 mA

LF156 Only

- High slew rate — 13 V/ μS
- Wide gain bandwidth — 8 MHz
- Fast settling time to 0.01% — 4 μS

LF 157 Only

- High slew rate — 60 V/ μS
- Wide bandwidth decompensated ($A_{\text{VCL}} = 5 \text{ min}$) — 28 MHz
- Fast settling time — 4 μS

Description

The LF156 series of JFET-input operational amplifiers feature low input bias currents and high slew rate. They are direct replacements for the industry standard LF155/156/157 types (except that pin 8 is used for internal post-package V_{OS} trimming, so pin 8 cannot be used for PC board trace routing). Only military temperature range devices are available.

The LF155 is a general-purpose device having lower internal power dissipation than the other two versions, and a slew rate of 5 V/ μS .

The LF156 has higher internal stage currents than the LF155, giving it a slew rate of 12 V/ μS . The LF156, like the LF155, is compensated for ac stability in unity-gain applications.

The LF157 decompensated version is the fastest member of the series, with a 45 V/ μS slew rate. The LF157 requires a minimum closed-loop gain configuration of +5 for ac stability.

Two accuracy grades are offered for each version; the "A" versions have tighter V_{OS} , I_{B} , and I_{OS} specifications. All types are offered in hermetic DIP, TO-99 can, and LCC packages, and can be ordered with Mil-Std-883, Level B processing.

Connection Information

**8-Lead
Dual In-Line Package
(Top View)**

65-03206A

**8-Lead
TO-99 Metal Can
(Top View)**

65-03205A

Pin	Function
1	Bal
2	-In
3	+In
4	-V _s
5	Bal
6	Out
7	+V _s
8	Int. Trim*

**20-Pad LCC
(Top View)**

65-02657A

Pin	Function	Pin	Function
1	NC	11	NC
2	Bal	12	Bal
3	NC	13	NC
4	NC	14	NC
5	-In	15	Out
6	NC	16	NC
7	+In	17	+V _s
8	NC	18	NC
9	NC	19	NC
10	-V _s	20	Int. Trim*

*This pin has no user function, but is connected to an internal trim network.

Ordering Information

Part Number	Package	Operating Temperature Range
LF155AD	D	-55°C to +125°C
LF156AD	D	-55°C to +125°C
LF157AD	D	-55°C to +125°C
LF155D	D	-55°C to +125°C
LF156D	D	-55°C to +125°C
LF157D	D	-55°C to +125°C
LF155AT	T	-55°C to +125°C
LF156AT	T	-55°C to +125°C
LF157AT	T	-55°C to +125°C
LF155AL	L	-55°C to +125°C
LF156AL	L	-55°C to +125°C
LF157AL	L	-55°C to +125°C

Notes:

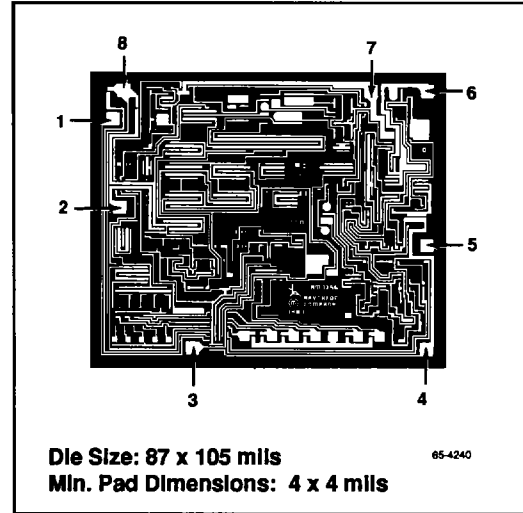
Add /883B suffix to basic part number to specify Mil-Std-883, Level B processing.
 L = 20-pad leadless chip carrier
 D = 8 lead ceramic DIP
 T = 8-lead metal can (TO-99)
 Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage	±22V
Differential Input Voltage Range	±40V
Input Voltage Range*	±20V
Output Short Circuit	Continuous
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Soldering Temperature (60 sec)	+300°C

*For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.

Mask Pattern



Thermal Characteristics

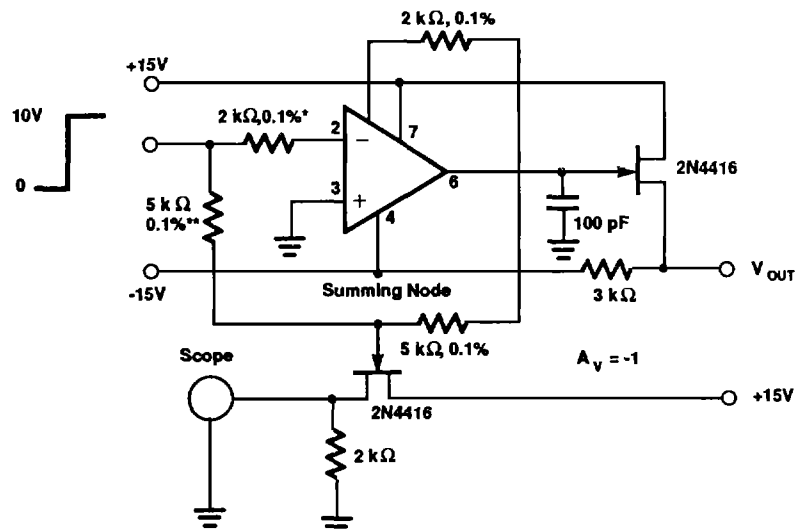
	8-Lead TO-99 Metal Can	8-Lead Ceramic DIP	20-Lead LCC Package
Max. Junction Temp.	175°C	175°C	175°C
Max. P_D $T_A < 50^\circ\text{C}$	658 mW	833 mW	925 mW
Therm. Res θ_{JC}	50°C/W	45°C/W	37°C/W
Therm. Res. θ_{JA}	190°C/W	150°C/W	105°C/W
For $T_A > 50^\circ\text{C}$ Derate at	5.26 mW/°C	8.33 mW/°C	7.0 mW/°C

Electrical Characteristics ($\pm 15V \leq V_S \leq \pm 20V$, $T_A = +25^\circ\text{C}$, unless otherwise noted)

Parameters	Test Conditions	LF155A/ 156A/157A		LF155/ 156/157		Units
		Min	Typ Max	Min	Typ Max	
Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$	0.3	2.0	0.4	5.0	mV
V_{OS} Adjustment Range		8.0		8.0		mV
Input Offset Current	$V_{CM} = 0V$, $T_J = +25^\circ\text{C}$	3	10	6	20	pA
Input Bias Current	$V_{CM} = 0V$, $T_J = +25^\circ\text{C}$	30	50	30	100	pA
Input Resistance		10^{12}		10^{12}		Ω
Large-Signal Voltage Gain	$V_S = \pm 15V$, $R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10V$	50	200	50	200	V/mV
Output Voltage Swing	$R_L = 10\text{ k}\Omega$, $V_S = \pm 15V$ $R_L = 2\text{ k}\Omega$, $V_S = \pm 15V$	± 12 ± 13.5 ± 10 ± 13.2		± 12 ± 13.5 ± 10 ± 13.2		V V
Supply Current	$V_S = \pm 15V$ LF155 LF156/157	3.0	4.0 4.0 7.0	3.0	4.0 4.0 7.0	mA mA
Slew Rate	$A_{VCL} = +1$, $V_S = \pm 15V$, LF155 $A_{VCL} = +1$, $V_S = \pm 15V$, LF156 $A_{VCL} = +5$, $V_S = \pm 15V$, LF157	3.0	6.0 10 13 40 60	2.0	6.0 7.5 13 30 60	V/ μS V/ μS V/ μS
Gain Bandwidth Product	$A_{VCL} = +1$, $V_S = \pm 15V$, LF155 $A_{VCL} = +1$, $V_S = \pm 15V$, LF156 $A_{VCL} = +5$, $V_S = \pm 15V$, LF157	6.0	8.0 30	5.7	7.6 28	MHz MHz MHz
Settling Time	T_O 0.01%, LF155 T_O 0.01%, LF156 T_O 0.01%, LF157	4.5	3.8 3.8	4.5	3.8 3.8	μS μS μS
Input Voltage Range	$V_S = \pm 15V$	± 10.5	± 15.1 -12.0	± 10.5	± 15.1 -12.0	V
Common Mode Rejection Ratio	$V_{CM} = \pm 10.5$	85	100	85	100	dB
Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$	85	100	85	100	dB
Input Noise Voltage Density	$R_S = 100\Omega$, $V_S = \pm 15V$ $F_O = 100\text{ Hz}$, LF155 $F_O = 1000\text{ Hz}$	25	20	25	20	nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
	$V_S = \pm 15V$ $F_O = 100\text{ Hz}$, LF156/157 $F_O = 1000\text{ Hz}$	15	12	15	12	nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Input Noise Current Density	$V_S = \pm 15V$ $F_O = 100\text{ Hz}$ $F_O = 1000\text{ Hz}$	0.01	0.01	0.01	0.01	pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$
Input Capacitance		3		3		pF

Electrical Characteristics ($\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted)

Parameters	Test Conditions	LF155A/ 156A/157A			LF155/ 156/157			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0\text{V}$	0.5	2.5		1.0	7.0		mV
Average Input Offset Voltage Drift	Without external trim, $R_S = 50\Omega$ With external trim, $R_S = 50\Omega$	3.0	5.0		5.0			$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
Input Offset Current	$T_J = +125^\circ\text{C}$, $V_{CM} = 0\text{V}$	0.6	10		0.8	20		nA
Input Bias Current	$T_J = +125^\circ\text{C}$, $V_{CM} = 0\text{V}$	10	25		10	50		nA
Input Voltage Range	$V_S = \pm 15\text{V}$	$\pm 10.4 + 15.1$ -12.0			$\pm 10.4 + 15.1$ -12.0			V
Common Mode Rejection Ratio	$V_S = \pm 15\text{V}$, $V_{CM} = \pm 10.4\text{V}$	85	100		85	100		dB
Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 20\text{V}$	85	100		85	100		dB
Large Signal Voltage Gain	$V_S = \pm 15\text{V}$, $R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	25	200		25	150		V/mV
Output Voltage Swing	$R_L \geq 10\text{k}\Omega$, $V_S = \pm 15\text{V}$ $R_L \geq 2\text{k}\Omega$, $V_S = \pm 15\text{V}$	$\pm 12 \pm 13.5$ $\pm 10 \pm 13.0$			$\pm 12 \pm 13.5$ $\pm 10 \pm 13.0$			V V

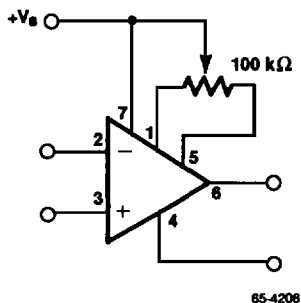


* $400\Omega \pm 0.1\%$ for LM157A

** $1\text{k}\Omega \pm 0.1\%$ for LM157A

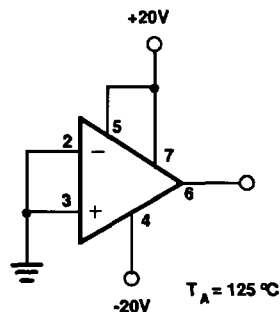
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Settling-Time Test Circuit



Note: For potentiometers with a temperature coefficient < 100 ppm/°C, the added TCV_{OS} with nulling is $\approx 0.5 \mu\text{V}/^\circ\text{C}/\text{mV}$ of adjustment

Input Offset Voltage Nulling



Burn-In Circuit

Applications Information

Input Voltage Considerations

The LF155/156/157 JFET input stages can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than $-V_S$ can result in a destroyed unit.

If both inputs exceed the negative common mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common mode voltage range.

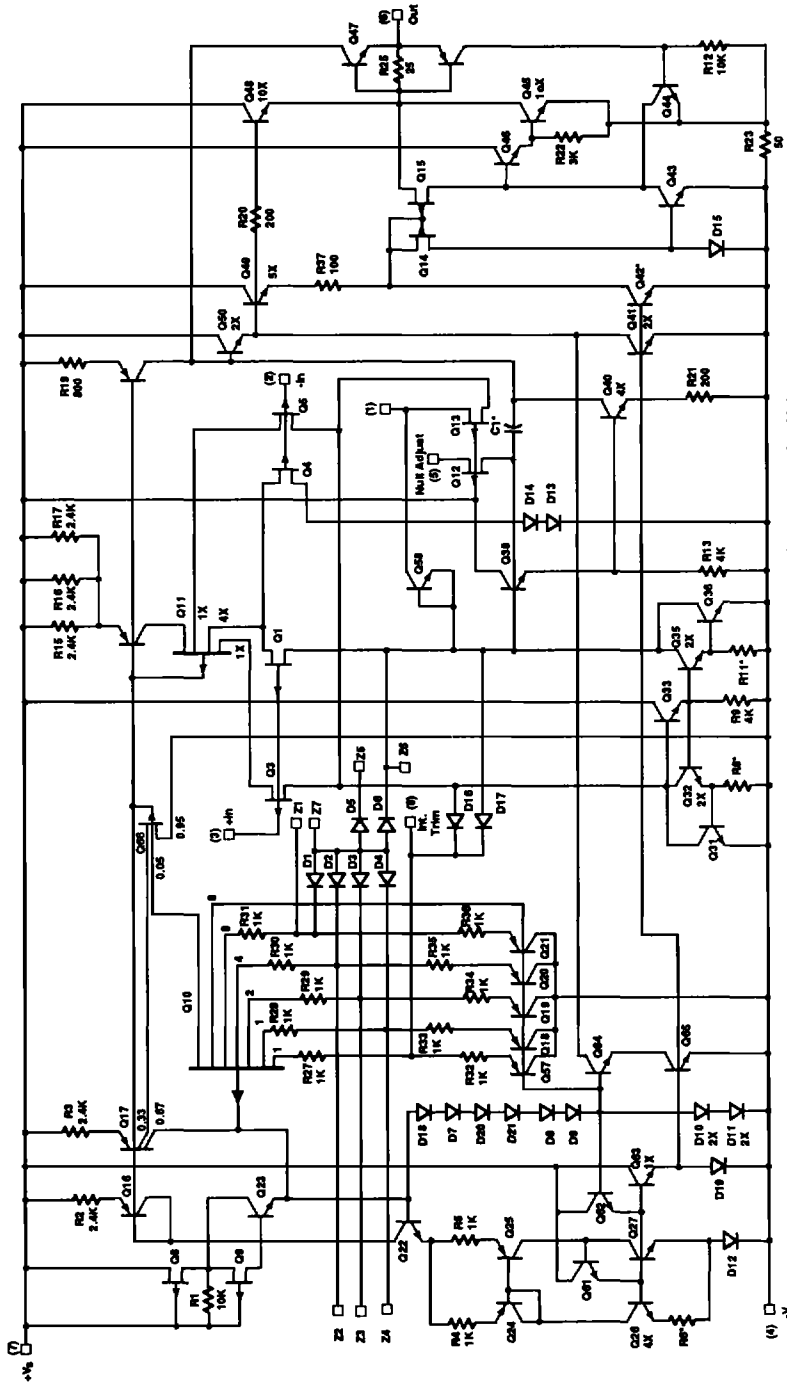
Exceeding the positive common mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

Dynamic Operation Considerations

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input. This minimizes "pick-up" and increases the frequency of the feedback pole by minimizing the capacitance from input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device to ac ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3 dB frequency of the closed-loop gain. Consequently, the pole has negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency, a lead capacitor should be placed from the output to the inverting input of the op amp. The capacitor value should be such that the RC time constant of the capacitor and feedback resistor is greater than, or equal to, the original feedback-pole time constant.

Schematic Diagram



* Table of Alternative Values

R8	R9	R11	Q42	C1
155	900	1.2K	2X	7 pF
156	480	900	4X	7 pF
157	480	900	4X	1.5 pF

Notes:
 1. All resistor values are in ohms.
 2. Pin numbers refer to DIP and TO-99 packages.