ISI IDEAL SEMICONDUCTOR INC.

"Your Best Defense Against Obsolescence"

259

54HCTLS
74HCTLS

OBJECTIVE SPECIFICATIONS

Features

- *8-Bit parallel-out storage register performs serial-to-parallel conversion with storage*
- *Asynchronous parallel clear*
- *Active high decoder*
- *Enable/Disable input simplifies expansion*
- *Expandable for N-bit applications*
- *Four distinct functional modes*
- *Function, pin-out, speed and drive compatability with 54/74LS logic family*
- *Low power consumption characteristic of CMOS*
- *High-Drive-Current outputs:* I_{OL} = 8 mA @ V_{OL} = 0.5V
- *Inputs and outputs interface directly with TTL, NMOS and CMOS devices*
- *Wide operating voltage range: 4.5V to 5.5V*
- *Characterized for operation over industial and military temperature ranges:*

  74HCTLS: -40°C to +85°C
  54HCTLS: -55°C to +125°C

Function Table

Inputs CLR	Inputs G	Output of Addressed Latch	Each Other Output	Function
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input.
Q_{i0} = the level of Q_i (i = Q, 1, ... 7, as appropriate) before indicated steady-state input conditions were established.

8-Bit Addressable Latches

Description

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of opration that are selected via the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unavvected by the data or address inputs.

In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

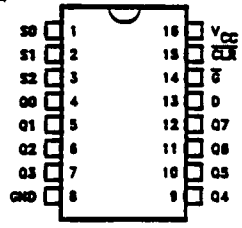
Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Latch Selection Table

Select Inputs S2	Select Inputs S1	Select Inputs S0	Latch Addressed
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

Pin Configuration



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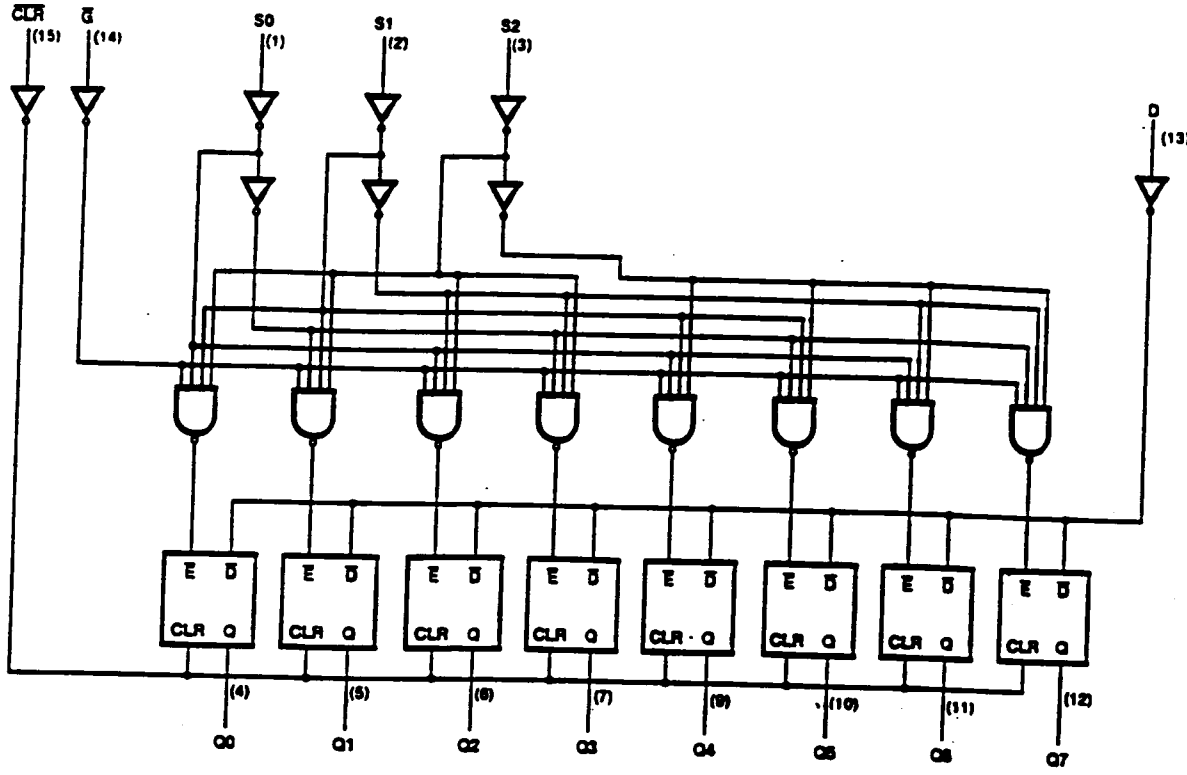
Logic Diagram



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Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} .....-05V to 7V
DC Input Diode Current, I_{IK}
(V_I <-0.5V or $V_I > V_{CC}$ + 0.5V) ..... ±20mA
DC Output Diode Current, I_{OK}
(V_O < -0.5V or $V_O > V_{CC}$ + 0.5V)..... ±20mA
Continuous Output Current Per Pin, I_O
(-0.5V < V_O < V_{CC} + 0.5V) ..... ±35mA
Continuous Current Through
V_{CC} or GND pins ..... ±125mA
Storage Temperature
Range, T_{STG} .....-65°C to +150°C
Power Dissipation Per Package, P_D•.....500mW

**Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.*

•Power Dissipation temperature derating:
Plastic Package (N): -12 mW/°C from 65°C to 85°C
Ceramic Package (J): -12 mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} .....4.5V to 5.5V
DC Input & Output Voltages, V_{IN} , V_{OUT} .....0V to V_{CC}*
Operating Temperature

Range — *74HCTLS: -40°C to +85°C*
54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f .....Max 500ns

**Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)*

DC Electrical Characteristics (V_{CC} = 5V ±10% Unless Otherwise Specified)

Sym	Parameter	Test Conditions	T_A = 25°C	74HCTLS T_A = -40°C to +85°C	54HCTLS T_A = -55°C to +125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_O = -20 µA I_O = -4 mA	V_{CC} 4.2	V_{CC} - 0.1 3.98	V_{CC} - 0.1 3.84	V_{CC} - 0.1 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{IH} or V_{IL} I_O = 20 µA I_O = 4 mA I_O = 8 mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA		8.0	80.0	160.0	µA

AC Electrical Characteristics (Input t_r, $t_f \leq 6$ ns), HCTLS259

Sym	Parameter		Conditions •	T_A = 25°C VCC - 5.0V	74HCTLS T_A = -40°C to +85°C V_{CC} = 5.0V ±10%		54HCTLS T_A = -55°C to +125°C V_{CC} = 5.0V ±10%	Unit
				Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to any Q		C_L = 50 pF	22	30	37	45	ns
t_{PLH}	Maximum Propagation Delay, Data to any Q			20	27	34	41	ns
t_{PHL}				20	27	34	41	
t_{PLH}	Maximum Propagation Delay, Address to any Q			26	34	43	51	ns
t_{PHL}				26	34	43	51	
t_{PLH}	Maximum Propagation Delay, $\overline{G}$ to any Q			22	30	37	45	ns
t_{PHL}				22	30	37	45	
t_w	Minimum Pulse Width	$\overline{CLR}$ Low		8	10	13	15	ns
		$\overline{G}$ Low		8	10	13	15	
t_{su}	Minimum Setup Time, Data or Address before $\overline{G}\uparrow$			8	10	13	15	ns
t_h	Minimum Hold Time, Data or Address after $\overline{G}\uparrow$			0	0	0	0	ns
C_{IN}	Maximum Input Capacitance			5				pF
C_{PD}	Power Dissipation Capacitance*			80				pF

*C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$

•For AC switching test circuits and timing waveforms see section 2.