FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through pin-out architecture**
- **Low inductance, multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16646 consist of 16 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both.The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16646DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16646DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 28	nDIR	Direction control input
2, 27	nCP_{AB}	Clock Input A-to-B
3, 26	nS_{AB}	Select input A-to-B
5, 6, 8, 9, 10, 12, 13, 14	$1A_0$ to $1A_7$	'1A' data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	$2B_0$ to $2B_7$	'2B' data inputs/outputs
29, 56	$n\overline{OE}$	Output enable
30, 55	nCP_{BA}	Clock input B-to-A
31, 54	nS_{BA}	Select input B-to-A
42, 41, 40, 38, 37, 36, 34, 33	$2B_0$ to $2B_7$	'2B' data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	$1B_0$ to $1B_7$	'1B' data inputs/outputs

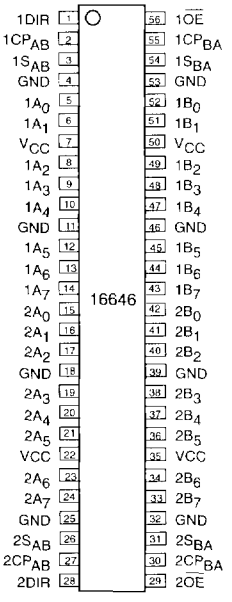


Fig.1 Pin configuration.

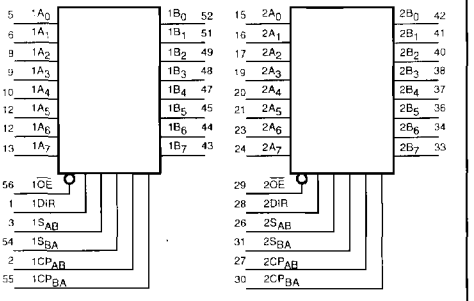


Fig.2 Logic symbol.

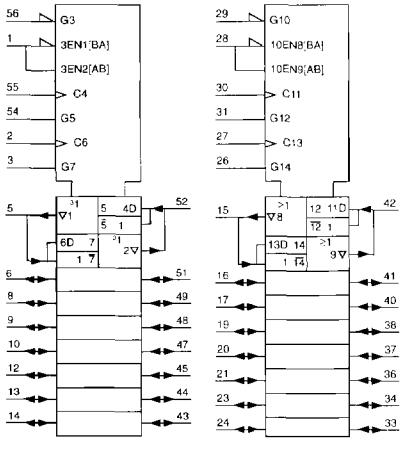


Fig.3 IEC logic symbol.

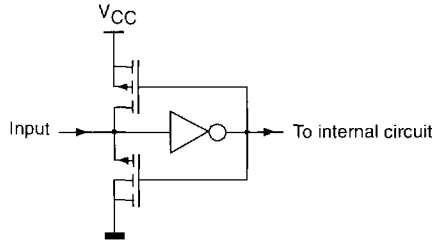


Fig.4 Bushold circuit

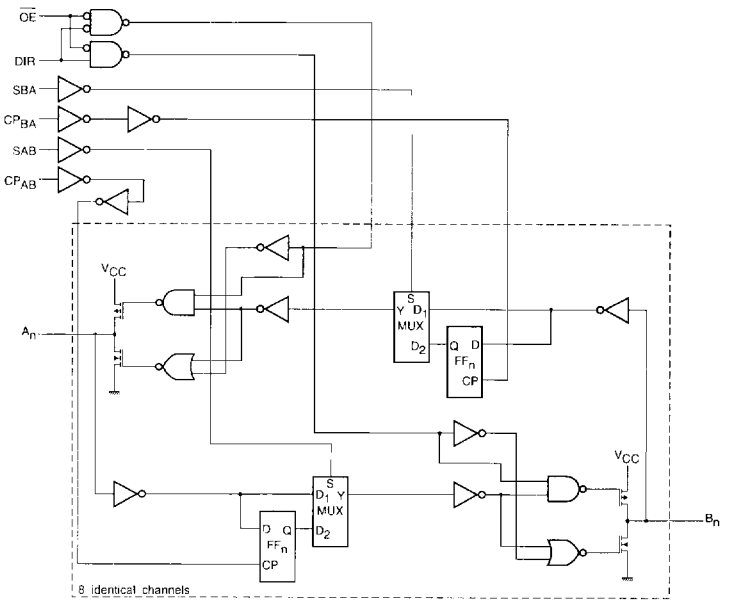


Fig.5 Logic diagram (one section)

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74ALVC16646

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16646

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	– – –	– – 3.0*	20.8 5.8 5.2	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	– – –	– – –	26.4 7.3 6.6	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	– – –	– – –	26.8 7.4 6.7	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n, B_n	– – –	– – –	20.7 7.2 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n, B_n	– – –	– – –	16.7 5.6 5.1	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n, B_n	– – –	– – –	23.5 7.5 6.8	ns	1.2 2.7 3.0 to 3.6	Fig.10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n, B_n	– – –	– – –	19.0 6.3 5.7	ns	1.2 2.7 3.0 to 3.6	Fig.10
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0 2.5	– –	– –	ns	2.7 3.0 to 3.6	Figs 7 and 8
t_{su}	set–up time A_n, B_n to CP_{AB}, CP_{BA}	– – 0.5	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	– – 0.5	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.7
f_{max}	maximum clock pulse frequency	180 200	– –	– –	ns	2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

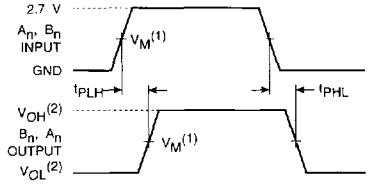


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delay times.

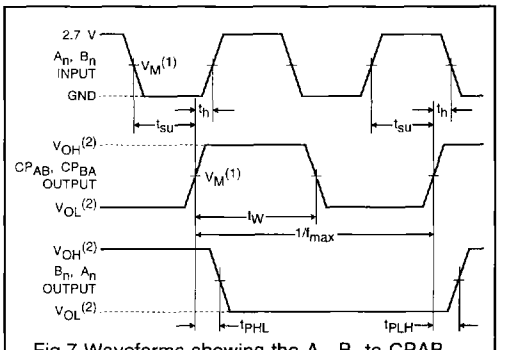


Fig.7 Waveforms showing the A_n, B_n to CPAB, CPBA set-up and hold times, clock CPAB, CPBA pulse width, maximum clock pulse frequency and the CPAB, CPBA to output B_n, A_n propagation delays.

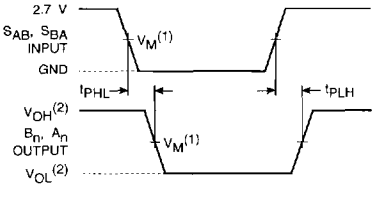


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times

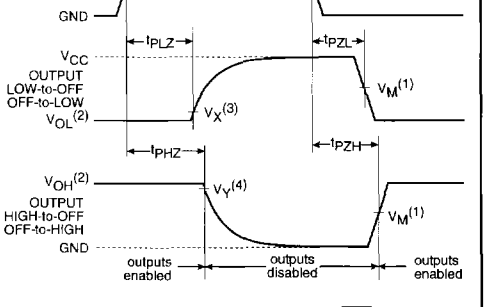


Fig.9 Waveforms showing the input $\overline{OE}$ to output A_n, B_n 3-state enable and disable times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = 0.9 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

AC WAVEFORMS
(Continued)

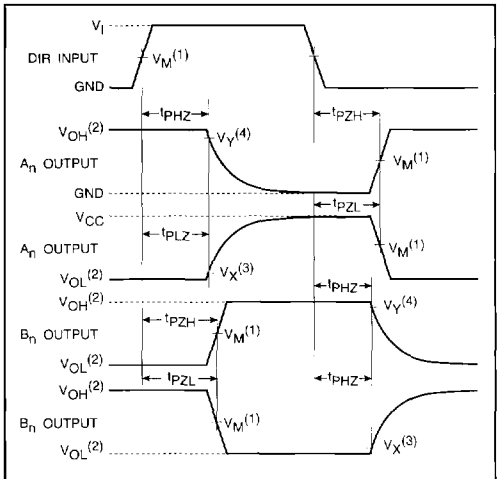
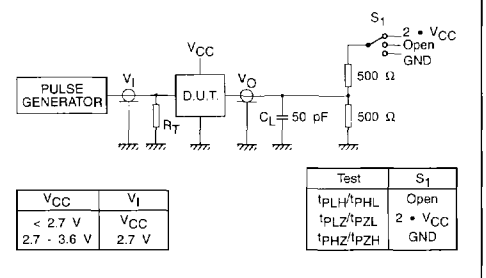


Fig.10 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.11 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

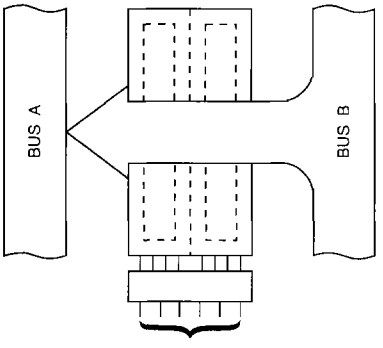
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(4) $V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

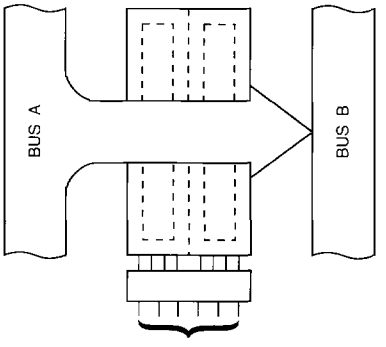
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



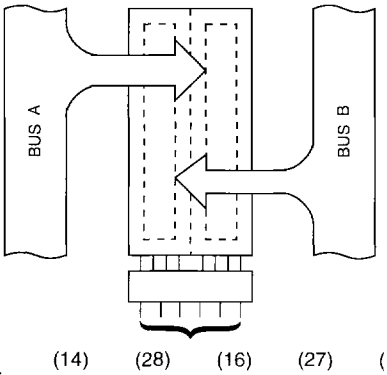
(1) $\overline{OE}$	(14) DIR	(28) CPAB	(16) CPBA	(27) SAB	(15) SBA
L	L	X	X	X	L

Real-time transfer; bus A to bus B



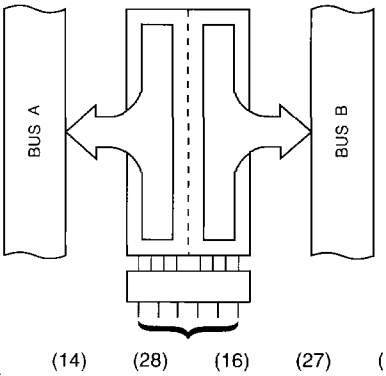
(1) $\overline{OE}$	(14) DIR	(28) CPAB	(16) CPBA	(27) SAB	(15) SBA
L	H	X	X	L	X

Storage from A, B or A and B



(1) $\overline{OE}$	(14) DIR	(28) CPAB	(16) CPBA	(27) SAB	(15) SBA
X	X	↑	X	X	
X	X	X	↑	X	
H	X	↑	↑	X	

Transfer storage data to A or B



(1) $\overline{OE}$	(14) DIR	(28) CPAB	(16) CPBA	(27) SAB	(15) SBA
L	X	H or L	X	H	L
L	H	H or L	X	H	X