Octal buffer/line driver (3-State) 54ABT541

FEATURES

- Octal bus interface
- Functions similar to the 4ABT241
- Provides ideal interface and increases fan-out of MOS Microprocessors
- Efficient pinout to facilitate PC board layout
- 3-State buffer outputs sink 48mA and source 24mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883C Method 3015.6 and 200V per Machine Model

DESCRIPTION

The 54ABT541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 54ABT541 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 48mA and sourcing 24mA. The device features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54ABT541/BRA
20-Pin FlatPack	54ABT541/BKA
20-Pin Ceramic LLCC	54ABT541/B2A

FUNCTION TABLE

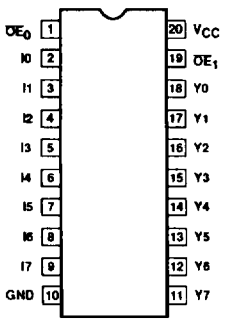
INPUTS			OUTPUT
$\overline{OE}_0$	$\overline{OE}_1$	I_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

PIN DESCRIPTION

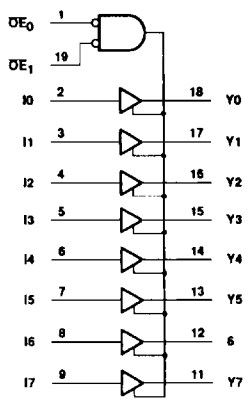
PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	In	Data inputs
18, 17, 16, 15, 14, 13, 12, 11	Yn	Data outputs
1, 19	$\overline{OE}_0$, $\overline{OE}_1$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

N and D Packages



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage range		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage range[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage range2	Output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	Output in Low state	128	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-55	+125	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = MAX, V_I = V_{IL} or V_{IH} unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -55 to +125°C		
			MIN	TYP[2]	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V, I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output to voltage	V_{CC} = 4.5V; I_{OH} = -3mA	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA	3.0			3.0		V
		V_{CC} = 4.5V; I_{OH} = -24mA	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 48mA		0.42	0.55		0.55	V
I_I	Input leakage current	V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_O = 2.7V		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_O = 0.5V		-5.0	-50		-50	µA
I_O	Short-circuit output current[4]	V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	Outputs High, V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		Outputs 3-State, V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[5]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

AC ELECTRICAL CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

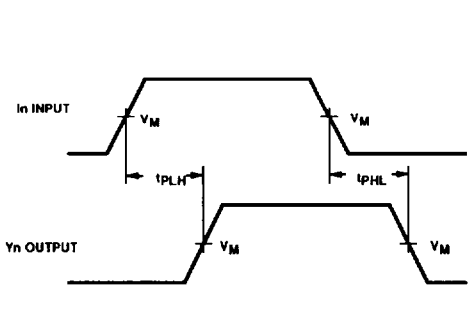
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55°C to +125°C, V_{CC} = +5.0V ± 0.5%		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Yb	Waveform 1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 2	1.1 2.1	3.1 4.4	4.8 5.9	1.1 2.1	5.3 6.4	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 2	2.1 1.7	5.1 4.7	6.6 6.2	2.1 1.7	7.1 6.7	ns ns

NOTES:

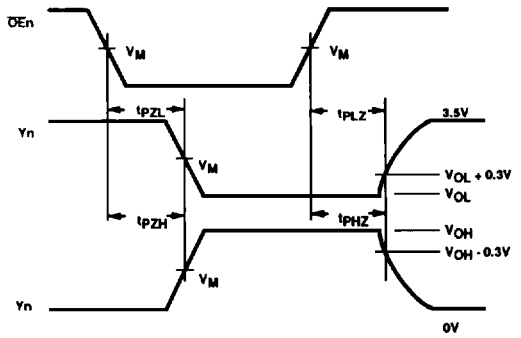
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. Not more than one output should be tested at a time, and the4 duration of the test should not exceed one second.
5. This is the increase in supply current for each input at 3.4V.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

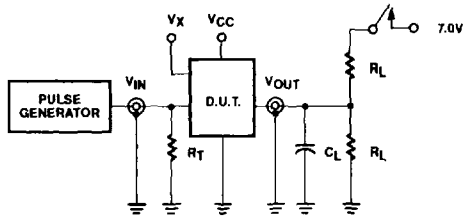


Waveform 1. Waveforms Showing the Input (In) to Output (Yn) Propagation Delays

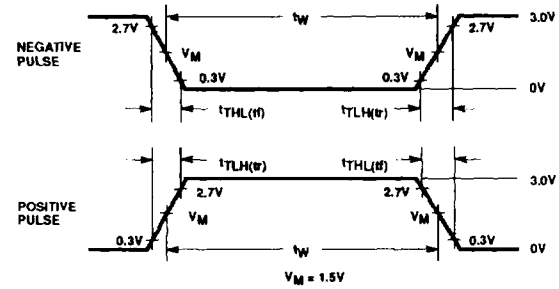


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definitions

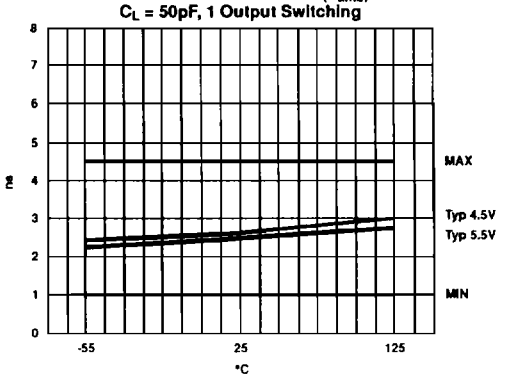
SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

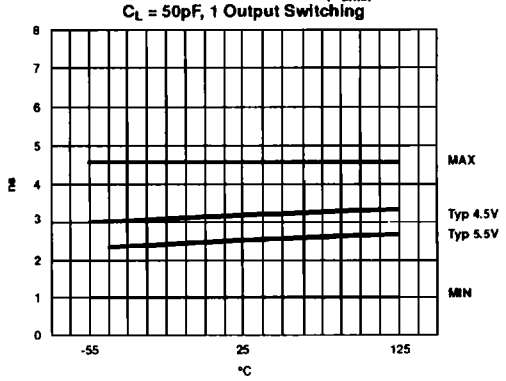
INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54ABT	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

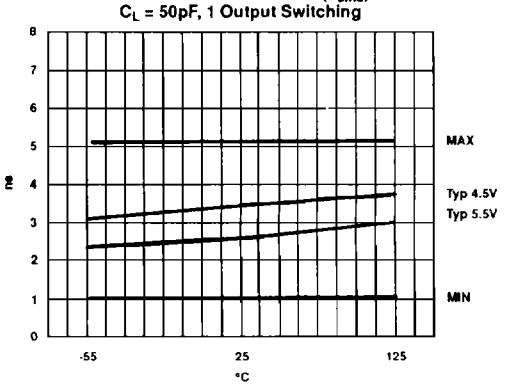
TPLH vs. TEMPERATURE (T_{amb})
C_L = 50pF, 1 Output Switching



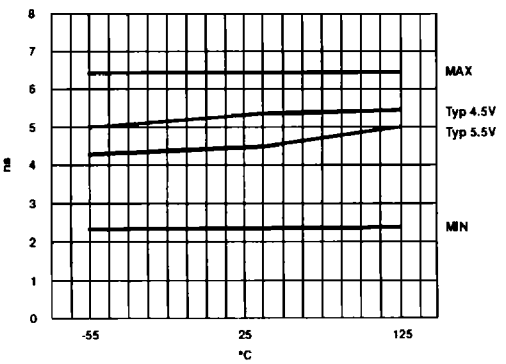
TPHL vs. TEMPERATURE (T_{amb})
C_L = 50pF, 1 Output Switching



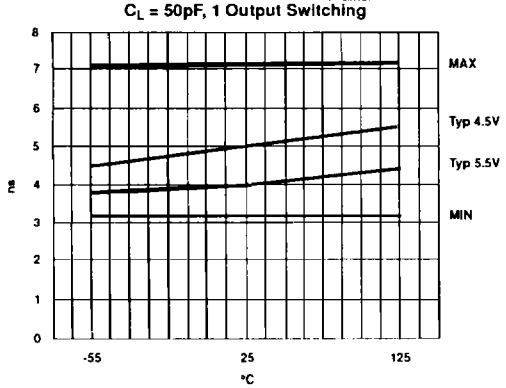
TPZH vs. TEMPERATURE (T_{amb})
C_L = 50pF, 1 Output Switching



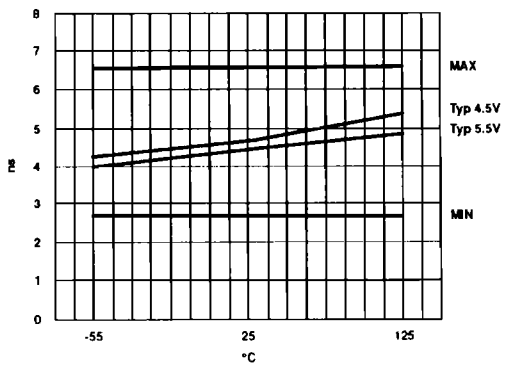
TPHZ vs. TEMPERATURE (T_{amb})
C_L = 50pF, 1 Output Switching



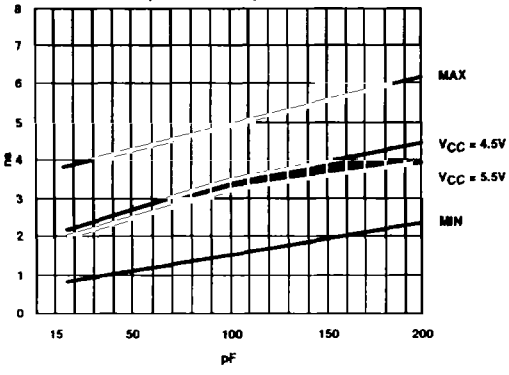
TPZL vs. TEMPERATURE (T_{amb})
C_L = 50pF, 1 Output Switching



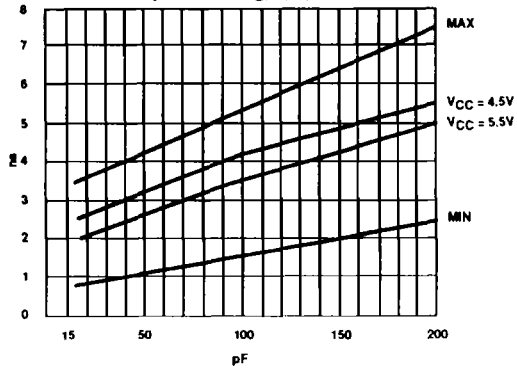
TPLZ vs. TEMPERATURE (T_{amb})
C_L = 50pF, 1 Output Switching



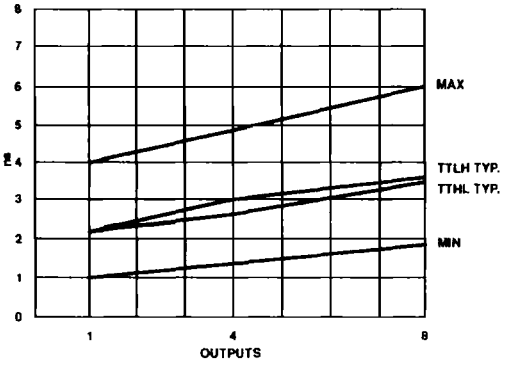
TPLH vs. LOAD CAPACITANCE[1]
1 Output Switching, T_{amb} = 25°C



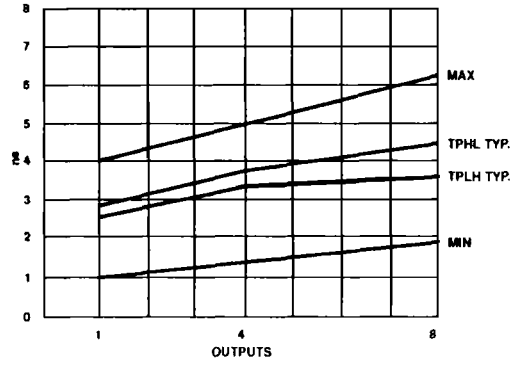
TPHL vs. LOAD CAPACITANCE[1]
1 Output Switching, T_{amb} = 25°C



TTLH TTHL vs. NUMBER OF OUTPUTS SWITCHING[1]
V_{CC} = 5.0V, T_{amb} = 25°C, C_L = 50pF

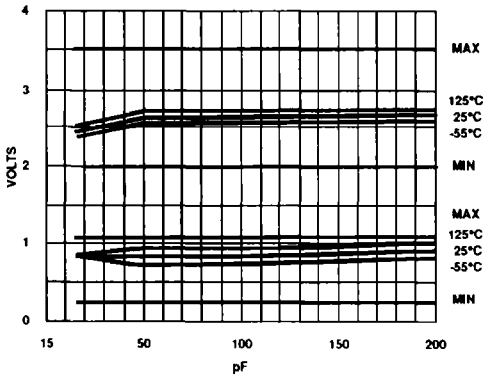


TPLH TPHL vs. NUMBER OF OUTPUTS SWITCHING[1]
V_{CC} = 5.0V, T_{amb} = 25°C, C_L = 50pF

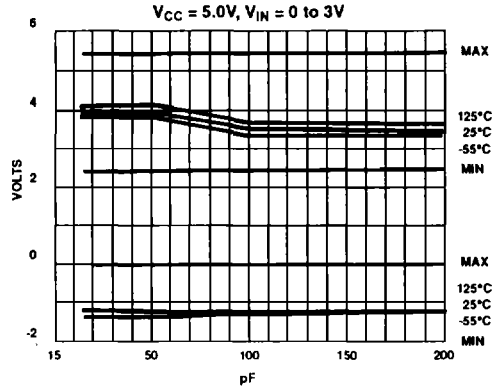


NOTE:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

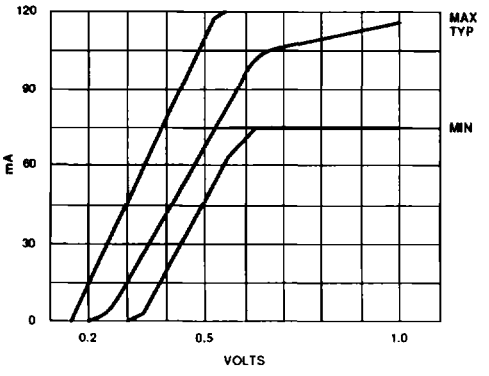
VOHV & VOLP[1] vs. LOAD CAPACITANCE[3]
V_{CC} = 5.0V, V_{IN} = 0 to 3V



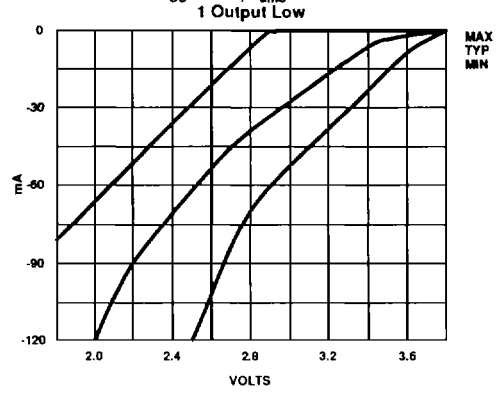
VOHV & VOLV[2] vs. LOAD CAPACITANCE[3]
V_{CC} = 5.0V, V_{IN} = 0 to 3V



VOL vs. IOL[3]
V_{CC} = 5.0V, T_{amb} = 25°C
1 Output Low



VOH vs. IOH[3]
V_{CC} = 5.0V, T_{amb} = 25°C
1 Output Low



NOTES:
1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.