LF356, LF356B, LF357*, LF357B*

MONOLITHIC JFET OPERATIONAL AMPLIFIERS

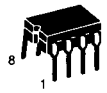
SILICON MONOLITHIC INTEGRATED CIRCUIT

Monolithic JFET Input Operational Amplifiers

These internally compensated operational amplifiers incorporate highly matched JFET devices on the same chip with standard bipolar transistors. The JFET devices enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

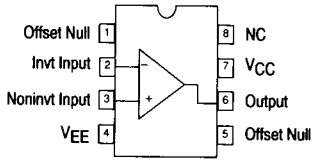
This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltage does not degrade the drift or common mode rejection.

- Low Input Bias Current: 30 pA
- Low Input Offset Current: 3.0 pA
- Low Input Offset Voltage: 1.0 mV
- Temperature Compensation of Input Offset Voltage: 3.0 μV/°C
- Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$
- High Input Impedance: $10^{12}\Omega$
- High Common Mode Rejection: 100 dB
- High DC Voltage Gain: 106 dB



J SUFFIX
CERAMIC PACKAGE
CASE 693

PIN CONNECTIONS



(Top View)

SERIES FEATURES

- LF356/356B: Wide Bandwidth
- LF357/357B: Wider Bandwidth Decompensated ($A_{V_{min}}$ = 5)

	LF356/356B	LF357/357B
Fast Setting Time to 0.01%	1.5 μs	1.5 μs
Fast Slew Rate	12 V/μs	50 V/μs
Wide Gain Bandwidth	5.0 MHz	20 MHz
Low Input Noise Voltage	12nV/$\sqrt{Hz}$	12nV/$\sqrt{Hz}$

APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

- Sample and Hold Circuits
- High Impedance Buffers
- Fast D/A and A/D Converters
- Precision High Speed Integrators
- Wideband, Low Noise, Low Drift Amplifiers

***NOTE:** The LF357/357B are designed for wider bandwidth applications. They are decompensated ($A_{V(min)}$ = 5).

ORDERING INFORMATION

Device	Temperature Range	Package
LF356BJ,J	0° to +70°C	Ceramic DIP
LF357BJ,J		Ceramic DIP

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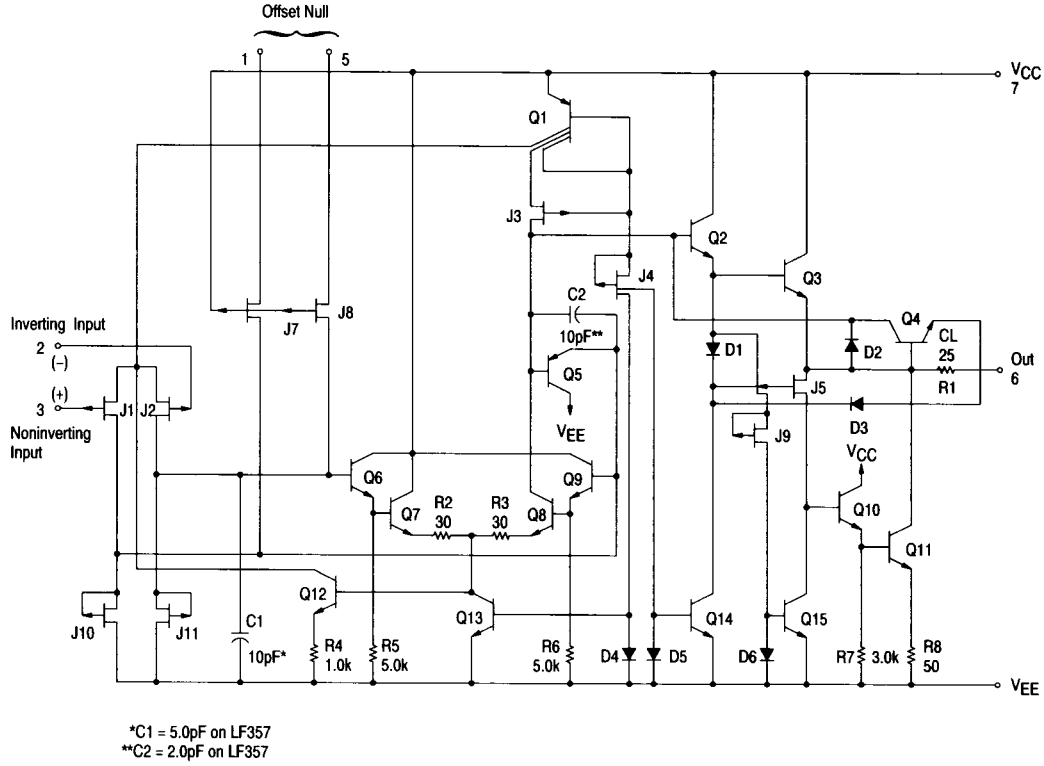
MAXIMUM RATINGS

Rating	Symbol	LF356B/357B	LF356/357	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	V
Differential Input Voltage	V_{ID}	±40	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±20	±16	V
Output Short Circuit Duration	T_{SC}	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70		°C
Operating Junction Temperature	T_J	150		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

NOTE: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

Circuit Schematic



*C1 = 5.0pF on LF357
**C2 = 2.0pF on LF357

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V to 20 V , V_{EE} = −15 V to −20 V for LF356B/357B; V_{CC} = +15 V, V_{EE} = −15 V for LF356/357; T_A = 0° to +70°C, unless otherwise noted.)

Characteristics	Symbol	LF356B/357B			LF356/357			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0) (T_A = 25°C) (Over Temperature)	V_{IO}	— —	3.0 —	5.0 6.5	— —	3.0 —	10 13	mV
Avg. Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\Delta V_{IO}/\Delta T$	—	5.0	—	—	5.0	—	μV/°C
Change in Average TC with V_{IO} Adjust (R_S = 50 Ω) (Note 2)	$\Delta TC/\Delta V_{IO}$	—	0.5	—	—	0.5	—	μV/°C per mV
Input Offset Current (V_{CM} = 0) (Note 3) (T_J = 25°C) ($T_J \leq$ 70°C)	I_{IO}	— —	3.0 —	2.0 1.0	— —	3.0 —	50 2.0	pA nA
Input Bias Current (V_{CM} = 0) (Note 3) (T_J = 25°C) ($T_J \leq$ 70°C)	I_{IB}	— —	30 —	100 5.0	— —	30 —	200 8.0	pA nA
Input Resistance (T_J = 25°C)	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k, V_{CC} = 15 V, V_{EE} = −15 V) (T_A = 25°C) (0°C ≤ T_A ≤ +70°C)	A_{VOL}	 50 25	 200 —	 — —	 25 15	 200 —	 — —	V/mV
Output Voltage Swing (V_{CC} = 15 V, V_{EE} = −15 V, R_L = 10 kΩ) (V_{CC} = 15 V, V_{EE} = −15 V, R_L = 2 kΩ)	V_O	±12 ±10	±13 ±12	— —	±12 ±10	±13 ±12	— —	V
Input Common Mode Voltage Range (V_{CC} = 15 V, V_{EE} = −15 V)	V_{ICR}	±11	+15.1 −12.0	—	±10	+15.1 −12.0		V
Common Mode Rejection	CMR	85	100	—	80	100	—	dB
Supply Voltage Rejection (Note 4)	PSR	85	100	—	80	100	—	dB
Supply Current (T_A = 25°C, V_{CC} = 15 V, V_{EE} = −15 V) LF356B/357B LF356/357	I_D	 —	 5.0 —	 7.0 —	 —	 — 5.0	 — 10	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LF356B/356			LF357B/357			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (Note 5) (A_V = 1) LF356 (A_V = 5) LF357	SR	7.5 —	12 —	— —	— 30	— 50	— —	V/μs
Gain Bandwidth Product	GBW	—	5.0	—	—	20	—	MHz
Settling Time to 0.01% (Note 6)	t_s	—	1.5	—	—	1.5	—	μs
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 100 Hz) (R_S = 100 Ω, f = 1000 Hz)	e_n	— —	15 12	— —	— —	15 12	— —	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 100 Hz) (f = 1000 Hz)	i_n	— —	0.01 0.01	— —	— —	0.01 0.01	— —	$pA/\sqrt{Hz}$
Input Capacitance	C_i	—	3.0	—	—	3.0	—	pF

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.
2. The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 μV/°C typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open-loop voltage gain are also unaffected by offset adjustment.
3. The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
4. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.
5. The minimum slew rate limits apply for the LF356B and the LF357B, but do not apply for the LF356 or LF357.
6. Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF356. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF357, A_V = −5.0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

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Figure 1. Input Bias Current versus Case Temperature

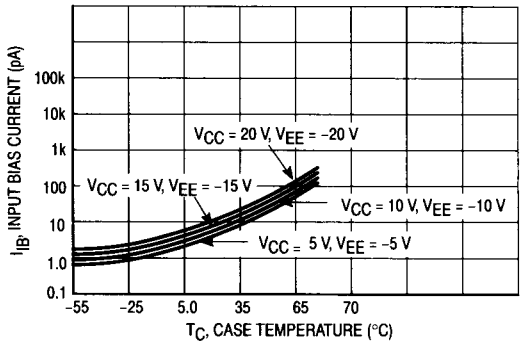

Figure 2. Input Bias Current versus Input Common Mode Voltage

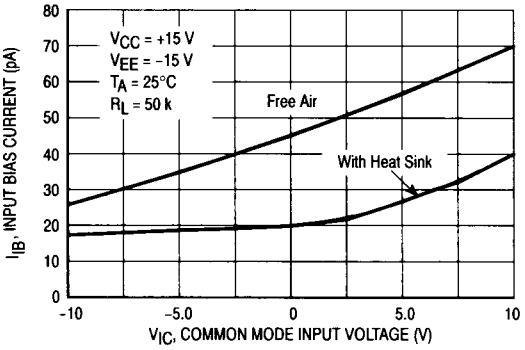

Figure 3. Output Voltage Swing versus Supply Voltage

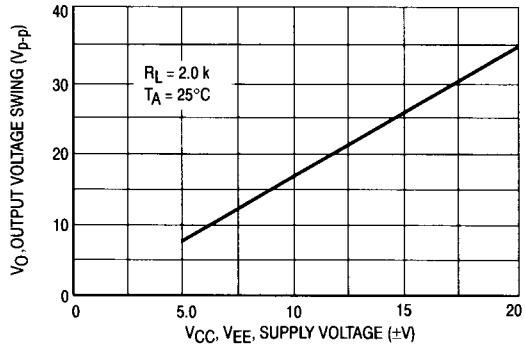

Figure 4. Supply Current versus Supply Voltage

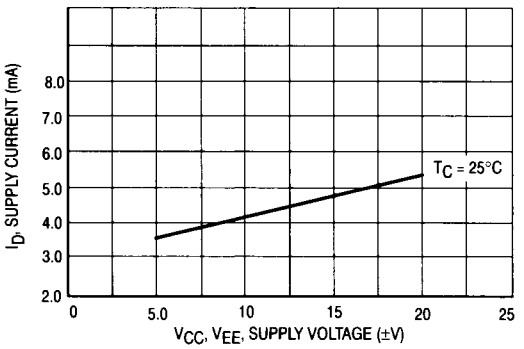

Figure 5. Negative Current Limit

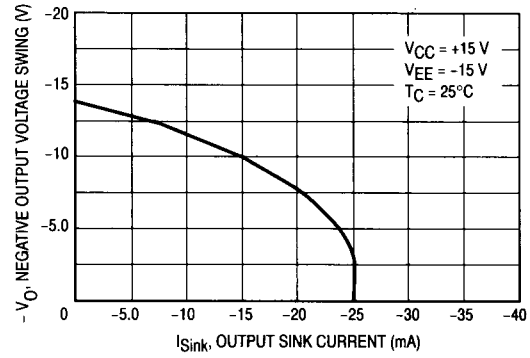

Figure 6. Positive Current Limit

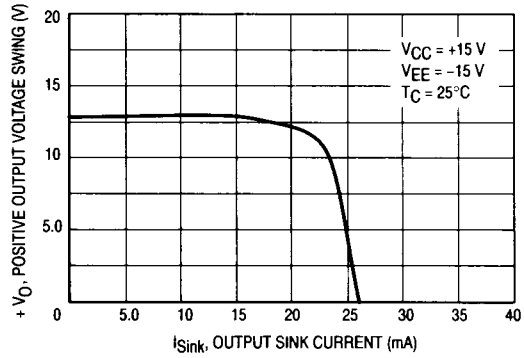

Figure 7. Positive Common Mode Input Voltage Limit

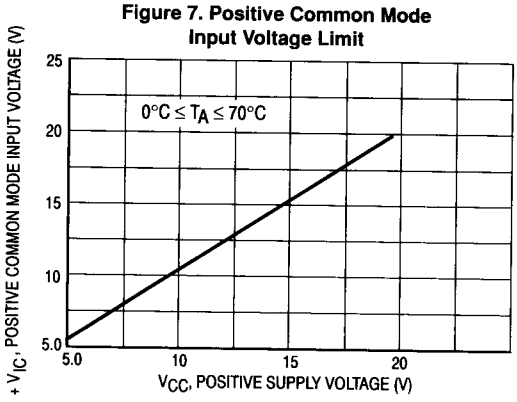

Figure 8. Negative Common Mode Input Voltage Limit

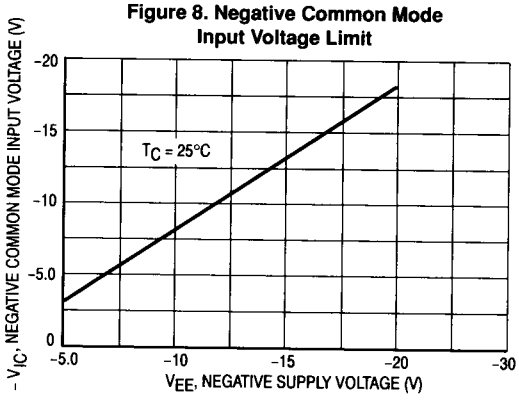

Figure 9. Open-Loop Voltage Gain

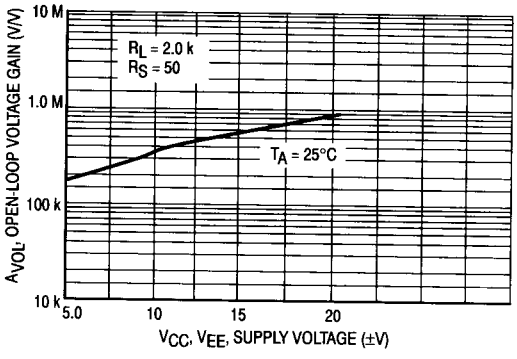

Figure 10. Output Voltage Swing versus Load Resistance

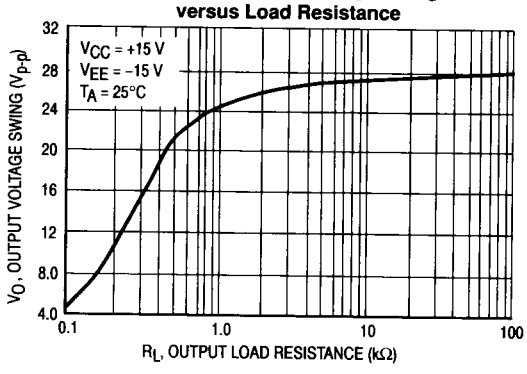

Figure 11. Gain Bandwidth Product (LF356 and LF357 Series)

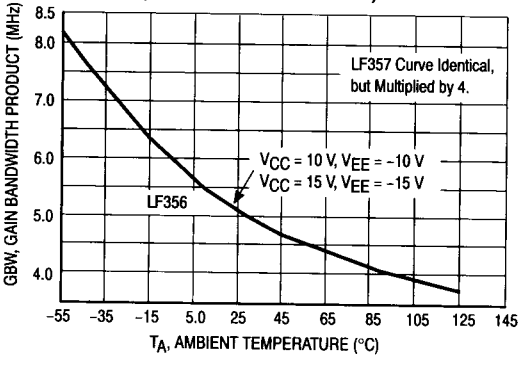

Figure 12. Inverter Settling Time (LF356 and LF357 Series)

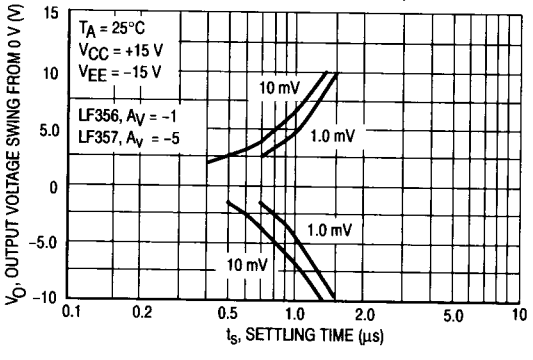

Figure 13. Normalized Slew Rate

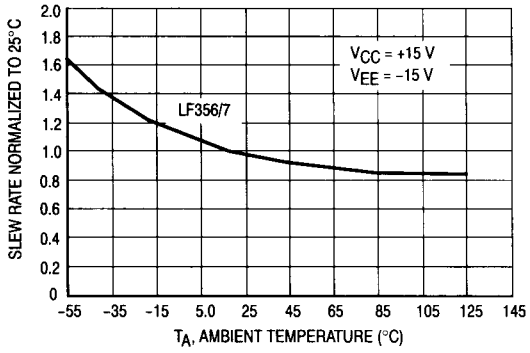

Figure 14. Open-Loop Frequency Response

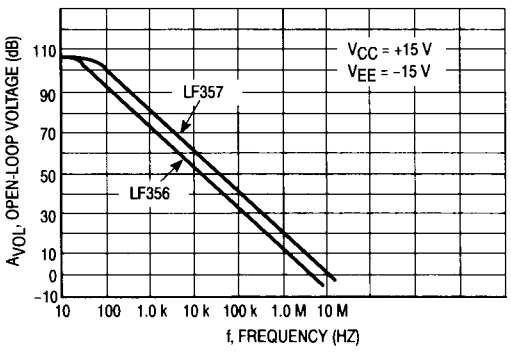

Figure 15. Bode Plot (LF356 Series)

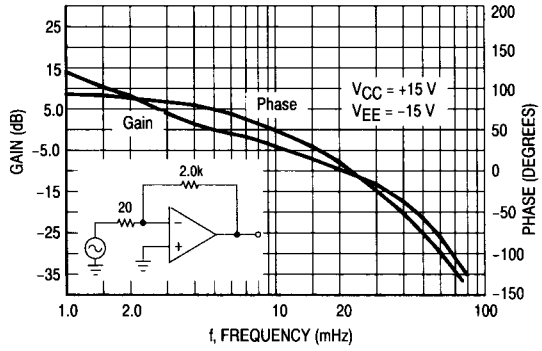

Figure 16. Output Impedance (LF356 Series)

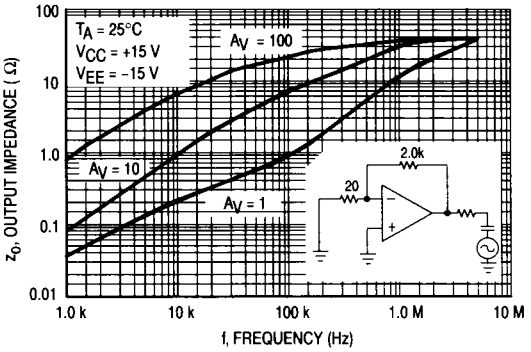

Figure 17. Bode Plot (LF357 Series)

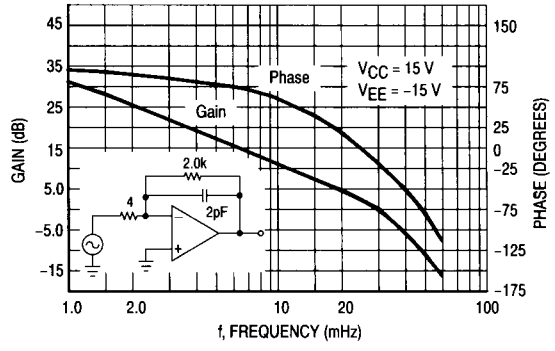

Figure 18. Output Impedance (LF357 Series)

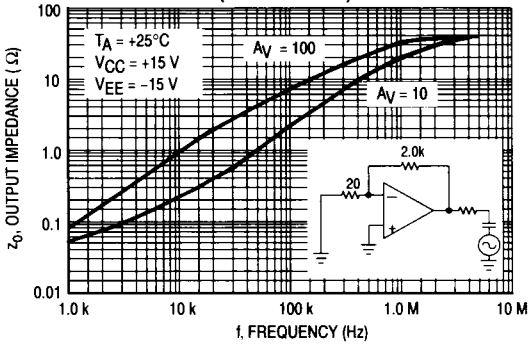

Figure 19. Common Mode Rejection Ratio

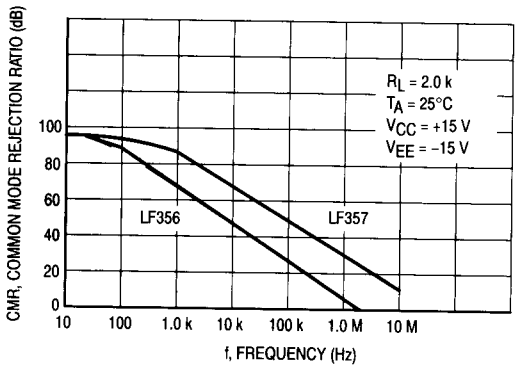

Figure 20. Undistorted Output Voltage Swing

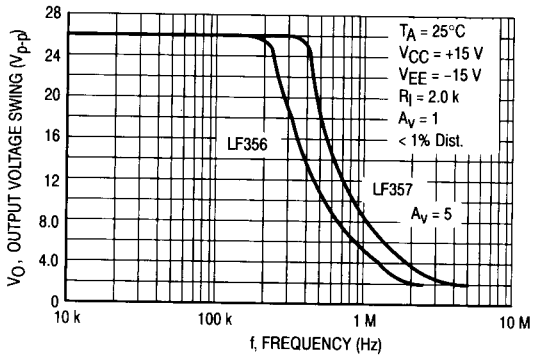

Figure 21. Power Supply Voltage Rejection Ratio

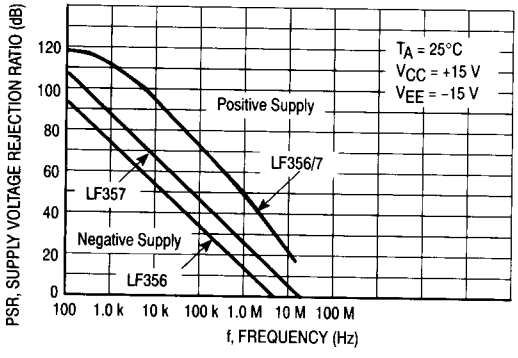

Figure 22. Equivalent Noise Voltage

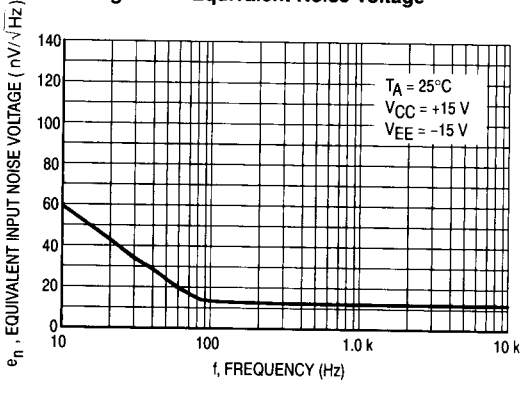

Figure 23. Equivalent Noise Voltage (Expanded Scale)

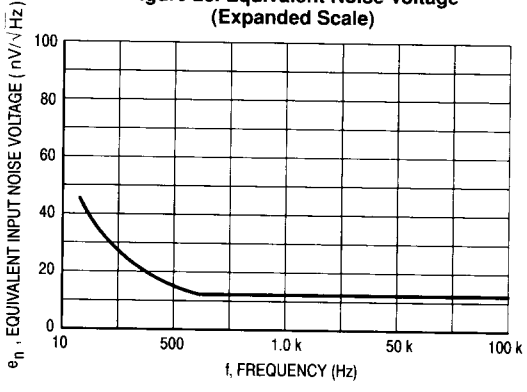

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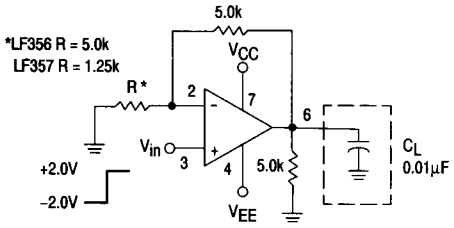
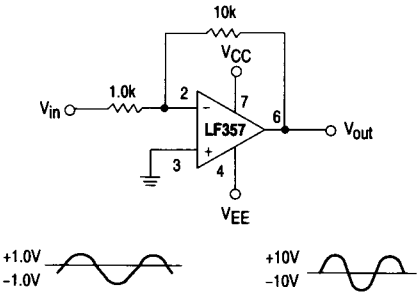
Figure 24. Driving Capacitive Loads



Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.

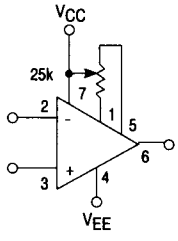
- $C_{L(max)} \cong 0.01\mu F$
- Overshoot $\leq$ 20%
- Settling time (t_s) $\cong$ 5.0 μs

Figure 25. Large Power Bandwidth Amplifier



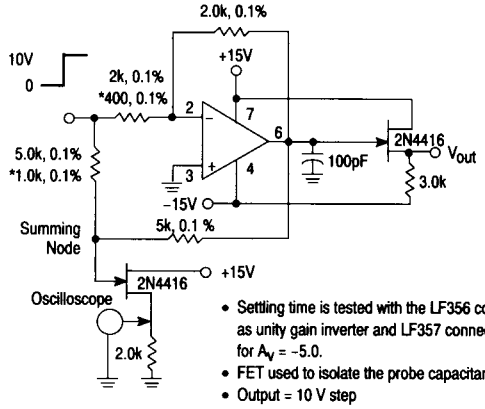
For distortion < 1% and a 20 Vp-p V_{out} swing, power bandwidth is 500 kHz.

Figure 26. Input Offset Voltage Adjustment



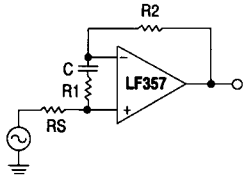
- V_{IO} is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to V_{CC}
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is $\approx$ 0.5 μV/°C/mV of adjustment.
- Typical overall drift: 5.0 μV/°C ±(0.5 μV/°C/mV of adjustment.)

Figure 27. Settling Time Test Circuit



- Settling time is tested with the LF356 connected as unity gain inverter and LF357 connected for A_V = -5.0.
- FET used to isolate the probe capacitance.
- Output = 10 V step
- A_V = -5.0 for LF357

Figure 28. Noninverting Unity Gain Operation



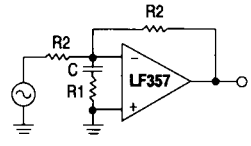
$$R1C \geq \frac{1}{(2\pi)\ (5.0\ MHz)}$$

$$R1 = \frac{R2 + R_S}{4}$$

$A_{V(DC)}$ = 1

$f_{-3dB} \approx$ 5.0 MHz

Figure 29. Inverting Unity Gain



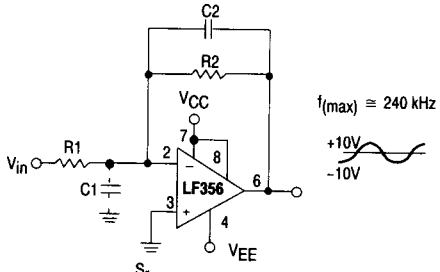
$$R1C \geq \frac{1}{(2\pi)\ (5.0\ MHz)}$$

$$R1 = \frac{R2}{4}$$

$A_{V(DC)}$ = -1

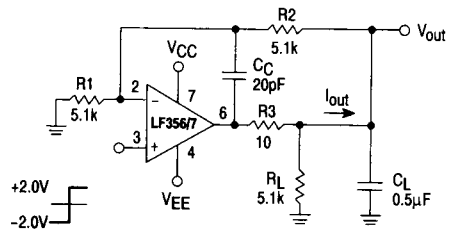
$f_{-3dB} \approx$ 5.0 MHz

Figure 30. Wide BW, Low Noise, Low Drift Amplifier



- Power BW: $f_{(max)} = \frac{S_r}{2\pi V_p} \cong 240\ kHz$
- Parasitic input capacitance (C1 ≅ 3.0 pF for LF356 and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

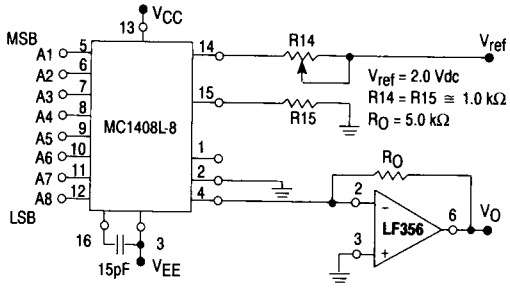
Figure 31. Isolating Large Capacitive Loads



- Overshoot 6%
- t_s = 10 µs
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

Figure 32. 8-Bit D/A with Output Current to Voltage Conversion



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 V.

$$V_O = \frac{2.0\ V}{1.0\ k}(5.0\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$