Signetics

54S112
Flip-Flop

Dual J-K Edge-Triggered Flip-Flop

Product Specification

Military Logic Products

DESCRIPTION

The 54S112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A High level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the High-to-Low transition of $\overline{CP}$.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54S112/BEA
16-Pin Ceramic FlatPack	54S112/BFA
16-Pin Ceramic LLCC	54S112/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

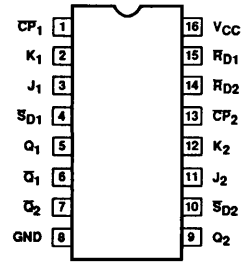
PINS	DESCRIPTION	54S
$\overline{CP}$	Clock input	2SUL
$\overline{R}_D$, $\overline{S}_D$	Reset and Set inputs	3.5SUL
J, K	Data inputs	1SUL
Q, $\overline{Q}$	Outputs	10SUL

NOTE: A 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

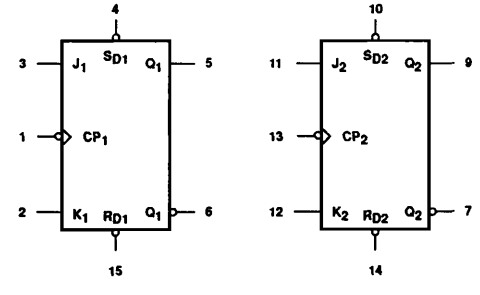
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +125	°C

PIN CONFIGURATION



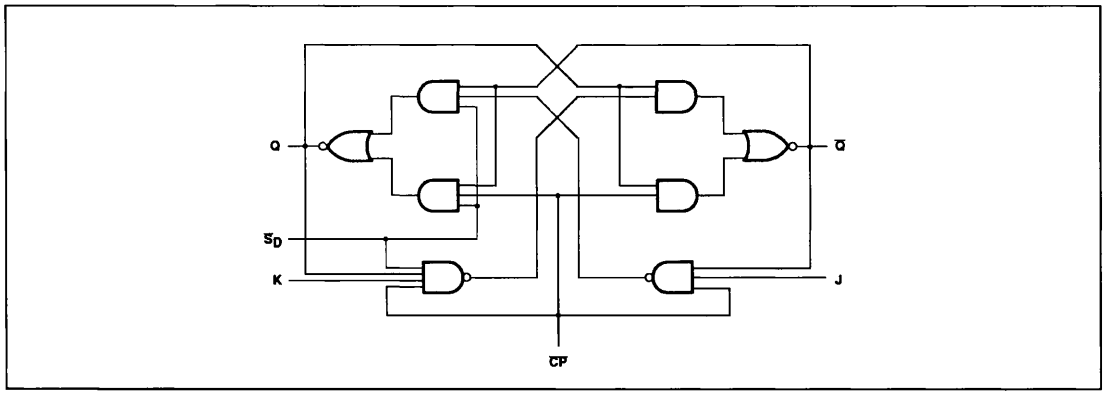
For LLCC Pin Assignment, see Jedec Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignment, see Jedec Standard No. 2

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = High voltage level steady state.
h = High voltage level one setup time prior to the High-to-Low Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the High-to-Low Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low Clock transition.
X = Don't Care.
↓ = High-to-Low Clock transition.

NOTE:
Both outpus will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
	+125°C			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1000	µA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max				0.5	V
			+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	J, K inputs			50	µA
			$\overline{R}_D$, $\overline{S}_D$ inputs			100	µA
			$\overline{CP}$ inputs			100	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	J, K inputs			-1.6	mA
			$\overline{R}_D$, $\overline{S}_D$ inputs			-7	mA
			$\overline{CP}$ inputs			-4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-110	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			15	50	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		7.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_D$ or $\overline{R}_D$ to output	Waveform 2		7.0 7.0	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_w(H)	Clock pulse width (High)	Waveform 1	6.0		ns
t_w(L)	Clock pulse width (Low)	Waveform 1	6.5		ns
t_w(L)	Set or reset pulse width (Low)	Waveform 2	8.0		ns
t_s	Setup time J or K to clock	Waveform 1	4.0		ns
t_h	Hold time J or K to clock	Waveform 1	0		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_D$ or $\overline{R}_D$ to output	Waveform 2		9.0 9.0	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

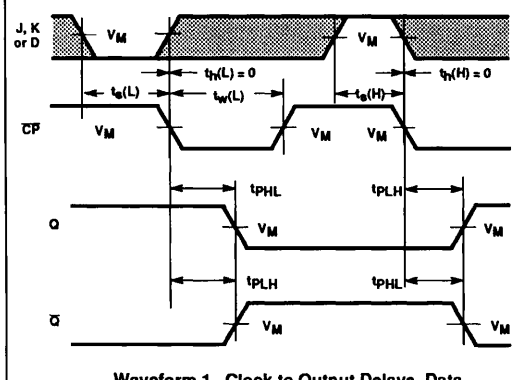
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	60		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		11.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_D$ or $\overline{R}_D$ to output	Waveform 2		11.0 11.0	ns ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

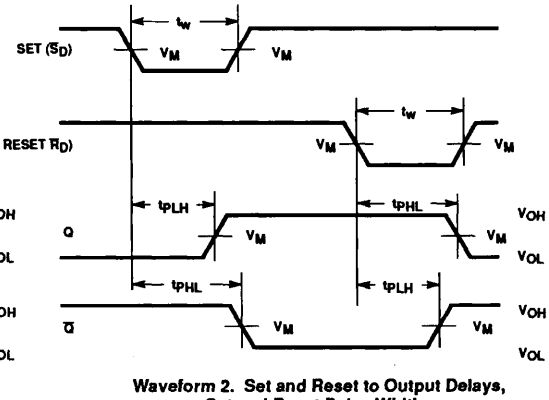
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_w(H)	Clock pulse width (High)	Waveform 1	10		ns
t_w(L)	Clock pulse width (Low)	Waveform 1	10		ns
t_w(L)	Set or reset pulse width (Low)	Waveform 2	10		ns
t_s	Setup time J or K to clock	Waveform 1	9.0		ns
t_h	Hold time J or K to clock	Waveform 1	2		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not0 tested.

AC WAVEFORMS



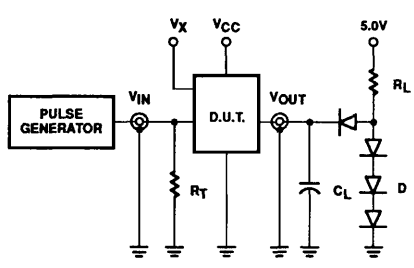
Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width



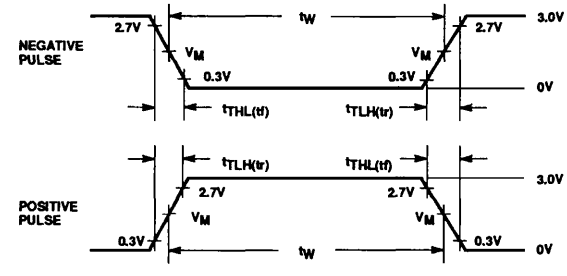
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths

NOTE: V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.