

Octal registered transceiver, inverting (3-State)

74ABT2953

FEATURES

- 8-bit registered inverting transceivers
- Separate clock, clock enable and 3-State enable provided for each register
- AM2953 functional equivalent
- Outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jeduc JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT2953 is an 8-bit registered inverting transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable (\overline{CEXX}) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable (\overline{OEXX}) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|------------------------|---|--|---------|------|
| | | $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$ | | |
| t_{PLH} t_{PHL} | Propagation delay CPAB or CPBA to $\overline{A_n}$ or $\overline{B_n}$ | $C_L = 50\text{pF}; V_{CC} = 5\text{V}$ | 5.0 | ns |
| C_{IN} | Input capacitance | $V_I = 0\text{V}$ or V_{CC} | 4 | pF |
| C_{OUT} | Output capacitance | $V_I = 0\text{V}$ or V_{CC} | 7 | pF |
| I_{CCZ} | Total supply current | Outputs Disabled; $V_{CC} = 5.5\text{V}$ | 500 | nA |

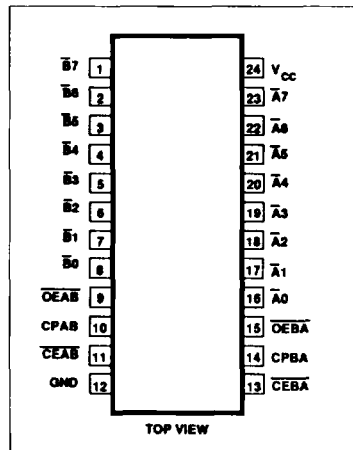
ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE |
|-----------------------------|-------------------|------------|
| 24-pin plastic DIP (300mil) | -40°C to +85°C | 74ABT2953N |
| 24-pin plastic SOL (300mil) | -40°C to +85°C | 74ABT2953D |

PIN DESCRIPTION

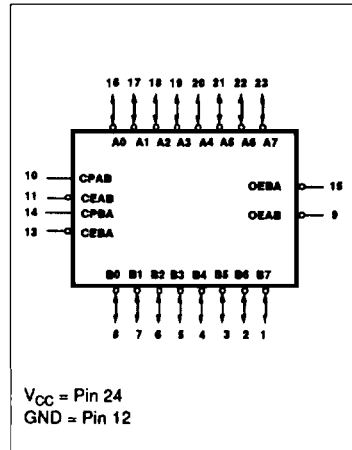
| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|----------------------------------|---------------------------------------|---|
| 10, 14 | CPAB / CPBA | Clock input A to B / Clock input B to A |
| 11, 13 | \overline{CEAB} / \overline{CEBA} | Clock enable input A to B / Clock enable B to A |
| 16, 17, 18, 19 20, 21, 22, 23 | $\overline{A_0} - \overline{A_7}$ | Data inputs/outputs (A side) |
| 1, 2, 3, 4 5, 6, 7, 8 | $\overline{B_0} - \overline{B_7}$ | Data inputs/outputs (B side) |
| 9, 15 | \overline{OEAB} / \overline{OEBA} | Output enable input |
| 12 | GND | Ground (0V) |
| 24 | V_{CC} | Positive supply voltage |

PIN CONFIGURATION DIP



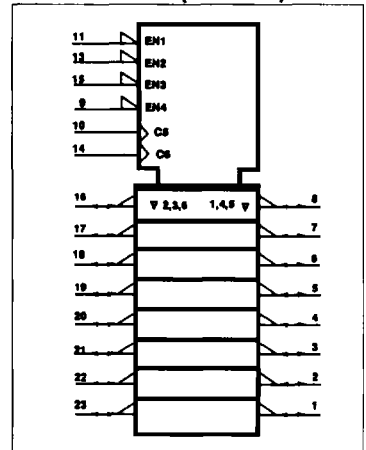
April 4, 1991

LOGIC SYMBOL



266

LOGIC SYMBOL (IEEE/IEC)



853-1555 02094

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FUNCTION TABLE for Register An or Bn

| An or Bn | INPUTS | | INTERNAL Q | OPERATING MODE |
|----------|--------|------|------------|----------------|
| | CPXX | CEXX | | |
| X | X | H | NC | Hold data |
| L | ↑ | L | L | Load data |
| H | ↑ | L | H | |

H= High voltage level

L= Low voltage level

↑ =Low-to-High transition

X=Don't care

XX=AB or BA

NC=No change

FUNCTION TABLE for Output Enable

| INPUTS | INTERNAL Q | An or Bn OUTPUTS | OPERATING MODE |
|--------|------------|------------------|-----------------|
| | | | |
| H | X | Z | Disable outputs |
| L | L | H | Enable outputs |
| L | H | L | |

H= High voltage level

L= Low voltage level

X=Don't care

XX=AB or BA

Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|------------------|--------------------------------|-----------------------------|--------------|------|
| V _{CC} | DC supply voltage | | -0.5 to +7.0 | V |
| I _{IK} | DC input diode current | V _I < 0 | -18 | mA |
| V _I | DC input voltage ³ | | -1.2 to +7.0 | V |
| I _{OK} | DC output diode current | V _O < 0 | -50 | mA |
| V _{OUT} | DC output voltage ³ | output in Off or High state | -0.5 to +5.5 | V |
| I _{OUT} | DC output current | output in Low state | 128 | mA |
| T _{stg} | Storage temperature range | | -65 to 150 | °C |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

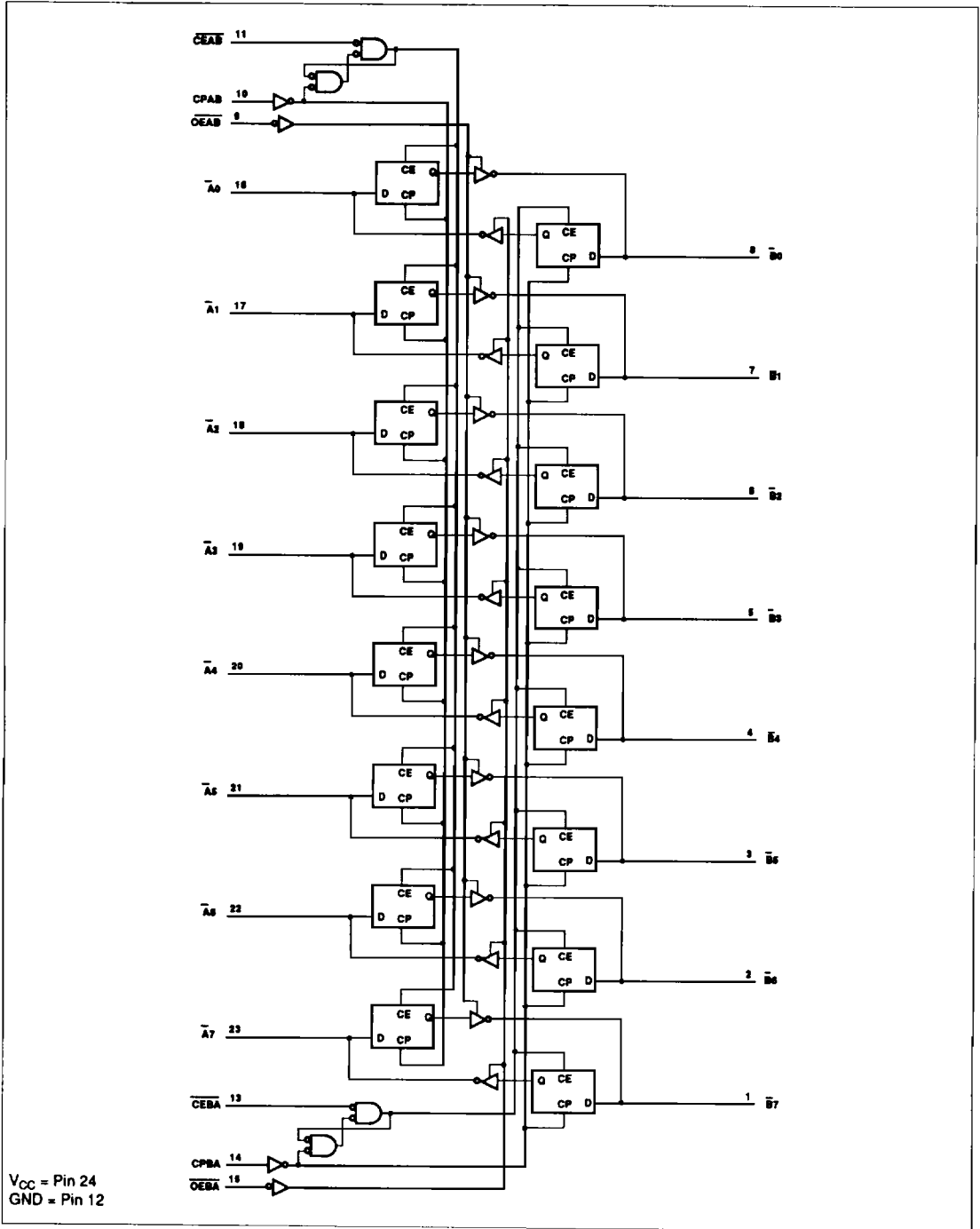
RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|------------------|--------------------------------------|--------|-----------------|------|
| | | Min | Max | |
| V _{CC} | DC supply voltage | 4.5 | 5.5 | V |
| V _I | Input voltage | 0 | V _{CC} | V |
| V _{IH} | High-level input voltage | 2.0 | | V |
| V _{IL} | Input voltage | | 0.8 | V |
| I _{OH} | High level output current | | -32 | mA |
| I _{OL} | Low level output current | | 64 | mA |
| ΔV/Δt | Input transition rise or fall rate | 0 | 10 | ns/V |
| T _{amb} | Operating free-air temperature range | -40 | +85 | °C |

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LOGIC DIAGRAM



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DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | | TEST CONDITIONS | LIMITS | | | | | UNIT |
|------------------------------------|--|--------------|--|--------------------------|-------|------|-----------------------------------|------|------|
| | | | | T _{amb} = +25°C | | | T _{amb} = -40°C to +85°C | | |
| | | | | Min | Typ | Max | Min | Max | |
| V _{IK} | Input clamp voltage | | V _{CC} = 4.5V; I _{IK} = -18mA | | -0.9 | -1.2 | | -1.2 | V |
| V _{OH} | High-level output voltage | | V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH} | 2.5 | 3.5 | | 2.5 | | V |
| | | | V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH} | 3.0 | 4.0 | | 3.0 | | |
| | | | V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH} | 2.0 | 2.6 | | 2.0 | | |
| V _{OL} | Low-level output voltage | | V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH} | | 0.42 | 0.55 | | 0.55 | V |
| I _I | Input leakage current | Control pins | V _{CC} = 5.5V; V _I = GND or 5.5V | | ±0.01 | ±1.0 | | ±1.0 | µA |
| | | Data pins | V _{CC} = 5.5V; V _I = GND or 5.5V | | 5 | 100 | | 100 | |
| I _{IH} + I _{OZH} | 3-State output High current | | V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH} | | 5.0 | 50 | | 50 | µA |
| I _{IL} + I _{OZL} | 3-State output Low current | | V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH} | | -5.0 | -50 | | -50 | µA |
| I _O | Short-circuit output current ¹ | | V _{CC} = 5.5V; V _O = 2.5V | -50 | -80 | -180 | -50 | -180 | mA |
| I _{CCH} | Quiescent supply current | | V _{CC} = 5.5V; Outputs High; V _I = GND or V _{CC} | | 0.5 | 50 | | 50 | µA |
| I _{CCL} | | | V _{CC} = 5.5V; Outputs Low; V _I = GND or V _{CC} | | 20 | 30 | | 30 | mA |
| I _{CCZ} | | | V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC} | | 0.5 | 50 | | 50 | µA |
| ΔI _{CC} | Additional supply current per input pin ² | | One input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V | | 0.3 | 1.5 | | 1.5 | mA |

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.

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AC ELECTRICAL CHARACTERISTICSGND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | UNIT |
|--------------------------------------|---|--------------------------|---|------------|------------|---|------------|------|
| | | | $T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = 5.0\text{V}$ | | | $T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = 5.0\text{V} \pm 0.5\text{V}$ | | |
| | | | Min | Typ | Max | Min | Max | |
| f_{MAX} | Maximum clock frequency | Waveform 1 | 150 | 200 | | 150 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay CPBA or CPAB to \bar{A}_n or \bar{B}_n | Waveform 1 | 2.0 2.5 | 5.1 5.7 | 6.6 7.2 | 2.0 2.5 | 7.6 8.2 | ns |
| t_{PZH} t_{PZL} | Output Enable time \bar{OEBA} or \bar{OEAB} to \bar{A}_n or \bar{B}_n | Waveform 3 Waveform 4 | 1.0 2.2 | 3.3 4.7 | 4.8 6.2 | 1.0 2.2 | 5.8 7.5 | ns |
| t_{PHZ} t_{PLZ} | Output Disable time \bar{OEBA} or \bar{OEAB} to \bar{A}_n or \bar{B}_n | Waveform 3 Waveform 4 | 2.0 1.5 | 6.1 5.6 | 7.6 7.1 | 2.0 1.5 | 8.1 7.6 | ns |

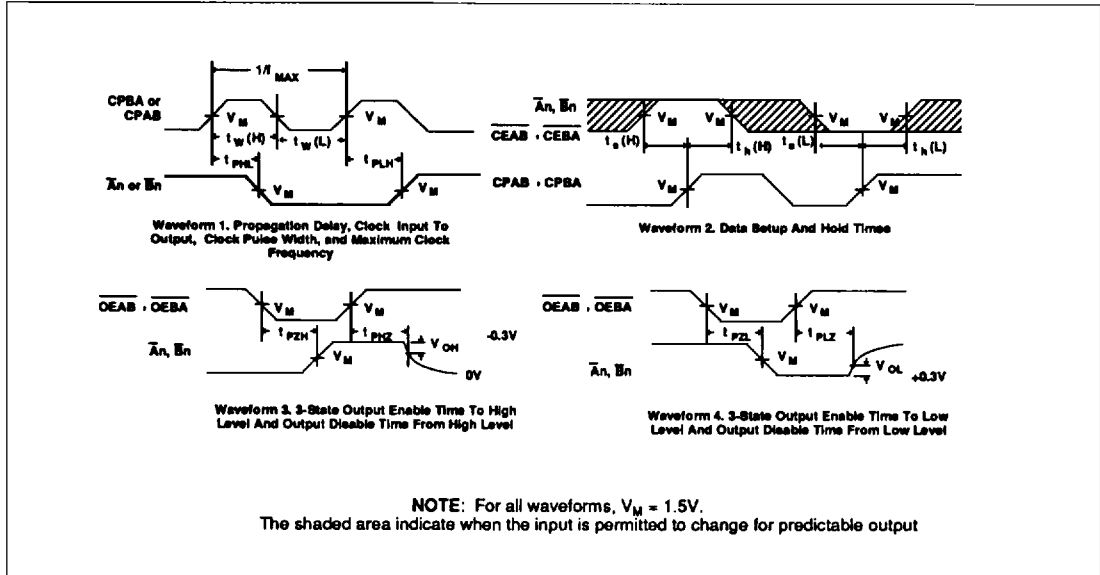
AC SETUP REQUIREMENTSGND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | UNIT |
|------------------------------------|---|----------------|---|--------------|-----|---|-----|------|
| | | | $T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = 5.0\text{V}$ | | | $T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = 5.0\text{V} \pm 0.5\text{V}$ | | |
| | | | Min | Typ | Max | Min | Max | |
| $t_s(\text{H})$ $t_s(\text{L})$ | Setup time, High or Low \bar{A}_n or \bar{B}_n to CPAB or CPBA | Waveform 2 | 4.0 3.0 | 2.5 1.5 | | 4.0 3.0 | | ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, High or Low \bar{A}_n or \bar{B}_n to CPAB or CPBA | Waveform 2 | 0.0 0.0 | -1.0 -2.0 | | 0.0 0.0 | | ns |
| $t_s(\text{H})$ $t_s(\text{L})$ | Setup time, High or Low \bar{CEAB}, \bar{CEBA} to CPAB, CPBA | Waveform 2 | 3.5 2.5 | 2.0 1.2 | | 3.5 2.5 | | ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, High or Low \bar{CEAB}, \bar{CEBA} to CPAB, CPBA | Waveform 2 | 0.0 0.0 | -1.0 -1.0 | | 0.0 0.0 | | ns |
| $t_w(\text{H})$ $t_w(\text{L})$ | CPAB or CPBA Pulse width, High or Low | Waveform 1 | 3.0 3.5 | 2.0 2.6 | | 3.0 3.5 | | ns |

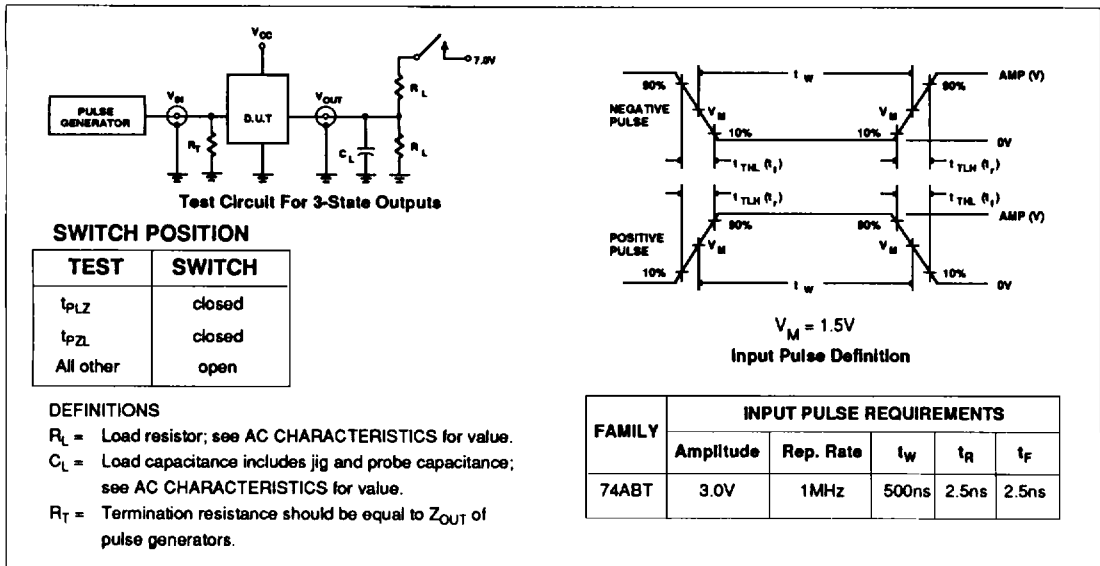
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AC WAVEFORMS

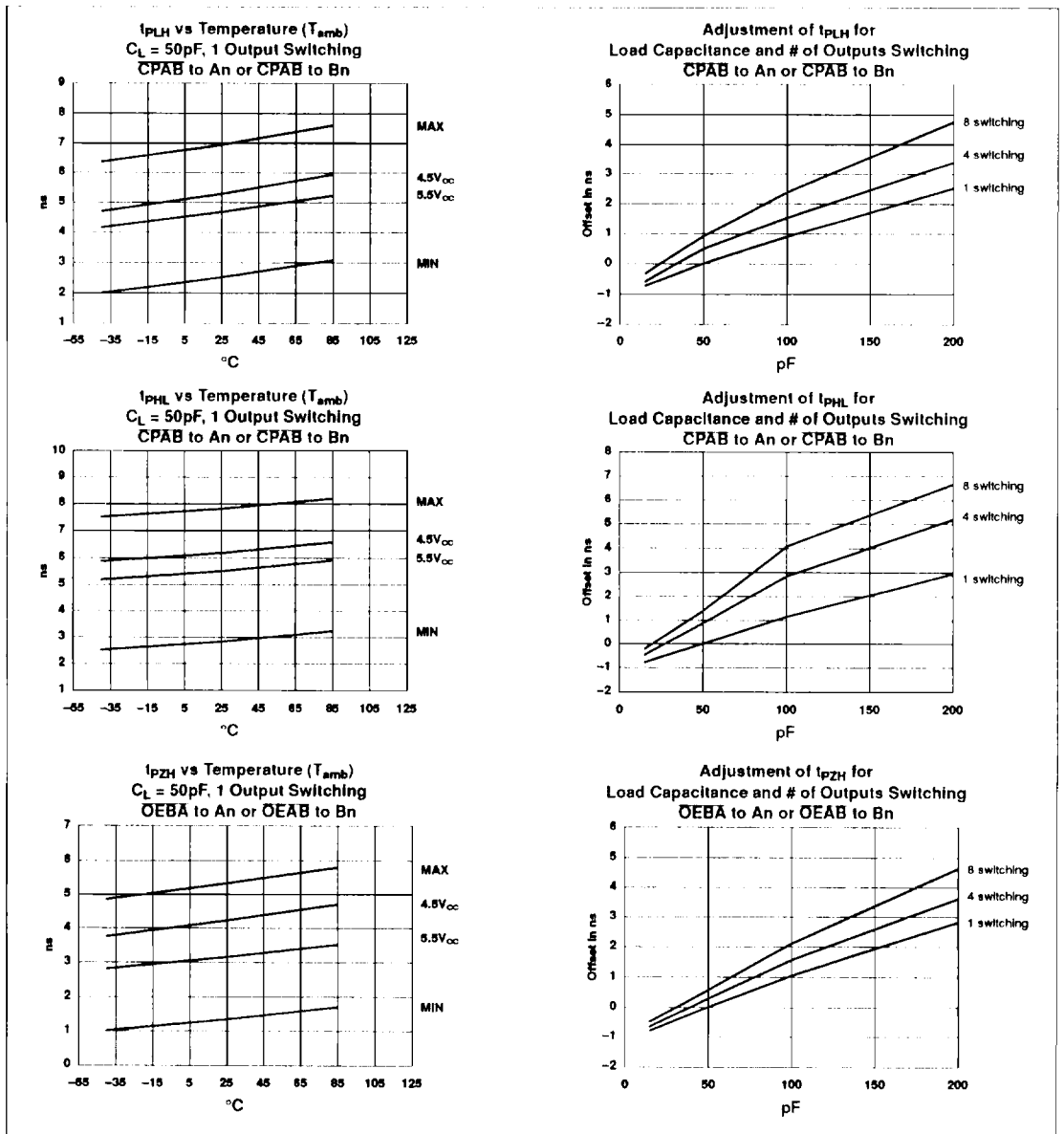


TEST CIRCUIT AND WAVEFORMS



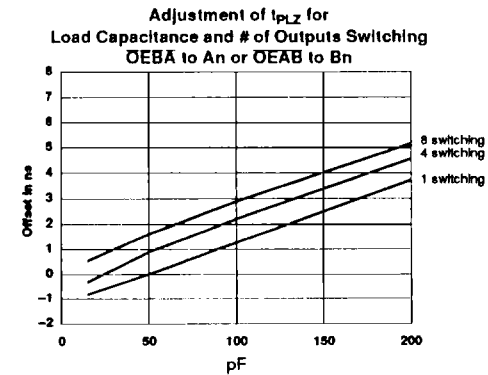
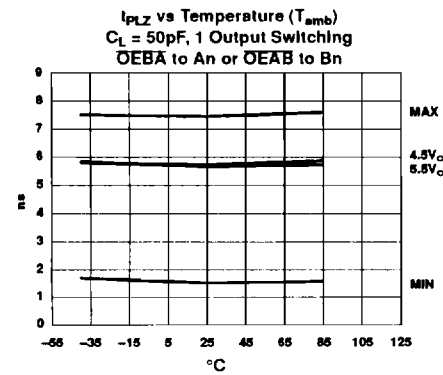
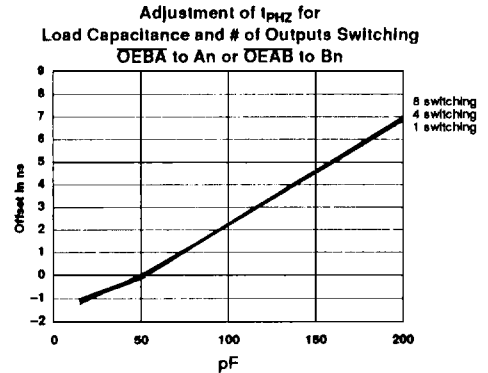
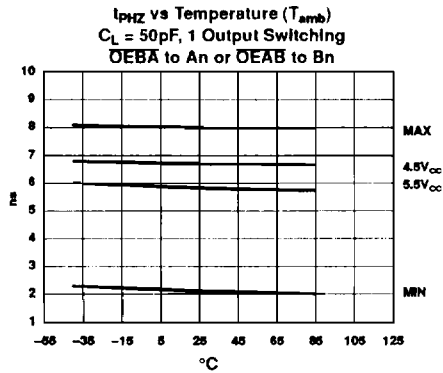
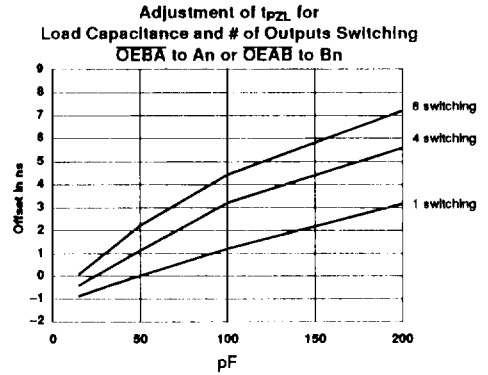
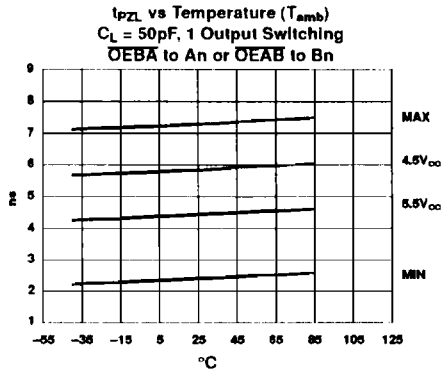
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